Design of an LVDS to USB3.0 adapter and application

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Abstract

USB 3.0 specification was published in 2008. With the development of technology, USB 3.0 is becoming popular. LVDS(Low Voltage Differential Signaling) to USB 3.0 Adapter connects the communication port of spectrometer device and the USB 3.0 port of a computer, and converts the output of an LVDS spectrometer device data to USB. In order to adapt to the changing and developing of technology, LVDS to USB3.0 Adapter was designed and developed based on LVDS to USB2.0 Adapter. The CYUSB3014, a new generation of USB bus interface chip produced by Cypress and conforming to USB3.0 communication protocol, utilizes GPIF-II(GPIF, general programmable interface) to connect the FPGA and increases effective communication speed to 2Gbps. Therefore, the adapter, based on USB3.0 technology, is able to connect more spectrometers to single computer and provides technical basis for the development of the higher speed industrial camera. This article describes the design and development process of the LVDS to USB3.0 adapter.

Keywords: USB3.0, LVDS, Communication adapter

Background

LVDS to USB3.0 Adapter is designed for ground-testing platform of satellite-borne DOAS(Differential Optical Absorption Spectroscopy) spectrometer. This spectrometer utilizes grating spectral optical path and 4 area array CCDs (Charge Coupled Device) to sense the optical spectrum signal of atmosphere in real-time and transforms this signal to digital data[1]. The structure of the spectrometer and satellite platform is shown in Fig.1.

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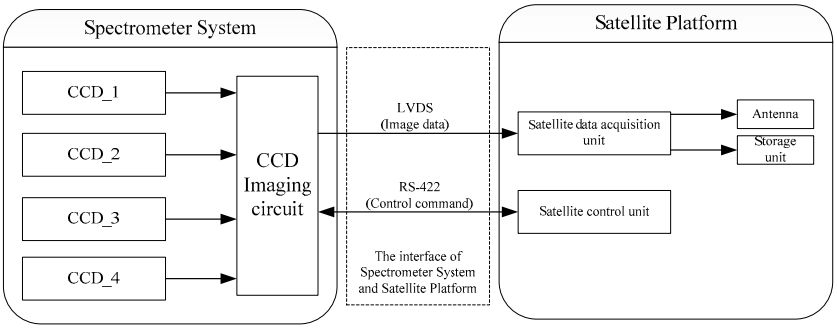

Fig.1 System scheme of spectrometer and satellite platform

It can be seen in Fig.1, the satellite platform connects spectrometer by RS-422 and LVDS communication line. Control commands, including exposure time and imaging modes, are sent to spectrometer by RS-422 communication line. At the same time, Spectrometer through the LVDS communication line sends the CCD image data to the satellite platform [2-3].

Because of satellite-borne DOAS spectrometer needs debugging and testing, including functional test, performance test and technical indicators test, in different environment, ground-testing platform must be researched and developed before spectrometer is completed. As can be seen in the Fig.2, the RS-422 interface transmits and receives command and the LVDS interface sends the image data to PC. However, LVDS interface cannot connect PC, because it is a special interface. Usually, Ground-testing platform utilizing data acquisition card to collect data and store data on PC[4]. However, Platform utilizing data acquisition card is so inconvenient. Nowadays, USB interface is a universal interface and very convenient for PC, which can solve the problem of other interfaces like single-function nature, bad data transmission reliability and not supporting hot plug. A LVDS to USB 2.0 Adapter has been developed and applied to Spectrometers.

Along with the developing of the technology, USB 3.0 is becoming popular. Comparing with USB 2.0, USB 3.0 provides higher speed up to 5 Giga bps[6]. Taking the advantage of the high speed, a LVDS-USB3.0 adapter is able to connect more spectrometers and multi-CCD spectrometers, which requires huge data transmision. Therefore, an LVDS to USB3.0 Adapter was developed. This article describes the design and development process of the adapter in detail.

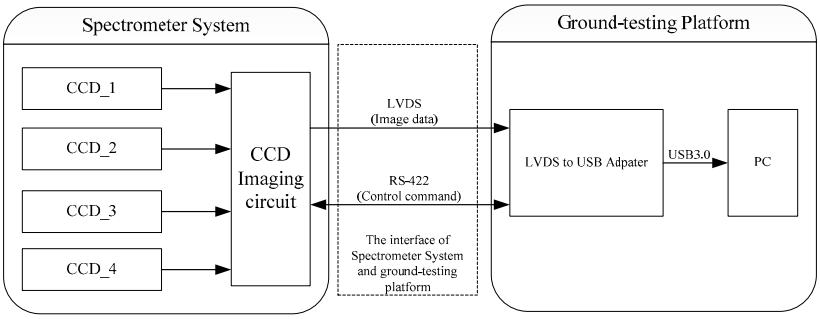

Fig.2 System scheme of spectrometer and ground-testing platform

1 System Design Method

1.1 Design of LVDS Interface

In this article, the LVDS consists of 3 differential signals, which are CS, SCK and SDA, as shown in Fig.3.

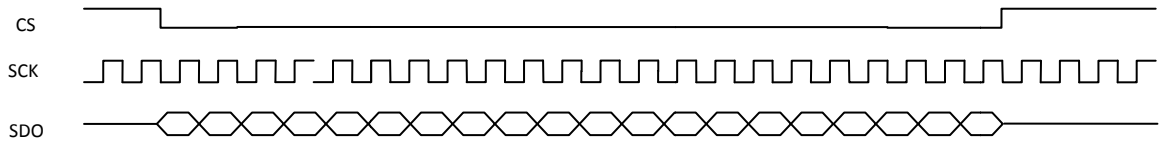

Fig.3 BUS timing diagram of SPI

When CS is low, data is valid and synchronously transmitted with clock. Each signal is transmitted using differential signaling. This bus rate can reach maximum 100Mbps when distance is shorter than 10m[7].

The LVDS data received by this system is 1024×1024×16bits, which consists of 1024 rows and each row includes 1024 pixels. Thus, the maxim data rate is 43Mbps with minimum exposure time(0.5s)[8]. In order to transmit data completely, the synchronous clock is applied to LVDS receiver and LVDS transmitter. Image data is valid when frame synchronous signal is valid.

The LVDS circuit consists of three parts: LVDS receiver, LVDS transmitter and LVDS connector. LVDS receiver convert balanced transmission LVDS signal to unbalanced transmission TTL signal. The LVDS interface circuit is shown in figure 4.

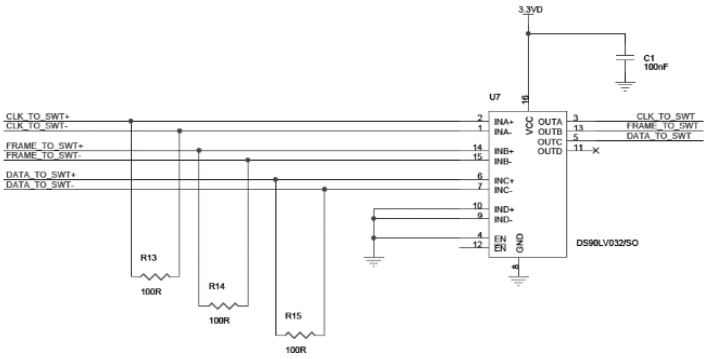

Fig.4 Diagram of LVDS circuit design

The input impedance of LVDS receiver is very high, according to IEEE, matched resistance is 100Ω, so most output current is flowed through the 100Ω resistance and causes about 350mV dropout at the receiver's input[7]. In this design, the receiver receives 3 pairs of differential signals: CLK_TO_SWT±、FRAME_TO_SWT± and DATA_TO_SWT±. They represent synchronous clock signal, frame synchronous signal and image data signal which converted to TTL by DS90lV032A.

1.2 Design of USB3.0 Interface

USB3.0 control chip applies to a CYUSB3014 which is a new generation of USB bus interface chip produced by Cypress. It conforms to USB 3.0 communication protocol, and backward compatible with USB2.0 communication protocol. This chip contains ARM926EJ-S and physical layer of USB3.0 and USB2.0. CYUSB3014 supports up to 16 input and 16 output interface and transmission speed can reach 5Gbps with Super-Speed mode[9]. However, because of PC operating system efficiency and communication redundancy, the actual rate is 2Gbps. In this design, the FPGA is applied for image data serial-parallel conversion and connects the CYUSB3014 with GPIF-II(GPIF, general programmable interface)[10]. Fig.5 shows this interconnect diagram between FPGA and USB.

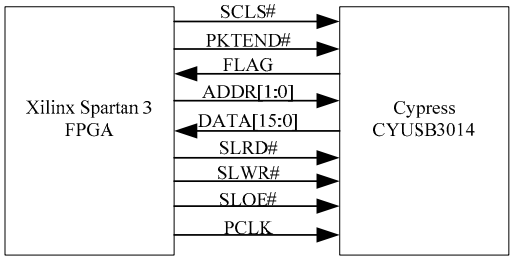

Fig.5 Interconnect Diagram between FPGA and USB

The USB signals description as shown in table 1.

Table 1 USB signals description

Signal Name	Signal Description
SCLS#	This is the chip select signal.
PKTEND#	This is the asserted to write packet.
FLAG	This is the index signal that indicate the availability of an CYUSB3014 socket.
ADDR[1:0]	This is the 2-bit address bus.
DATA[15:0]	This is the 16-bit data bus.
SLRD#	This is the read strobe signal.
SLWR#	This is the write strobe signal.
SLOE#	This is the output enable signal.
PCLK	This is the interface clock from FPGA.

1.3 Design of System

Based on the requirements of design, LVDS to USB3.0 adapter need to complete 2 function:

(1)The LVDS data, from spectrometer, are converted to USB data, and then send it to PC.

(2)The PC sends commands, such as exposure time, gain, image mode, etc, which are converted to synchronous serial data of RS-422 by adapter, and then the adapter sends it to spectrometer.

According to the above requirements, LVDS to USB3.0 Adapter hardware circuit include LVDS deserializer, data caching and USB interface. The structure of system design are shown in Fig.6.

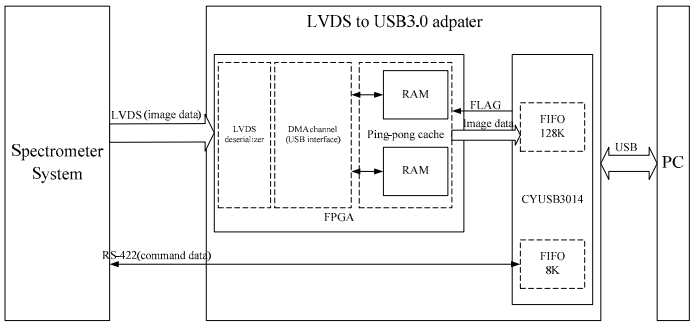

Fig. 6 Diagram of system design

When FPGA receives the frame image data, from spectrometer system by LVDS interface, the FPGA converts it to 16 bit parallel data. After 16 bit parallel data through Ping-pong cache, CYUSB3014 receives image data which will be sent to USB endpoint through inner DMA channel of CYUSB3014 as a Slave FIFO mode device. PC being able to send command to RS-422 interface of spectrometer system by USB interface is because USB interface supports Carkit UART mode for non-USB serial data transfer. When configured for the Carkit UART mode, TXD of UART(output) is mapped to the D- line, and RXD of UART (input) is mapped to the D+ line[10].

2 Design Implementation

2.1 FPGA Logical Control

The FPGA in this design is Xilinx chip XC3S400-208 which has 400K gate and 120 I/O[11]. The FPGA is mainly responsible for serial-parallel conversion of the LVDS signal, data buffering and time sequence logical control of CYUSB3014. The FPGA serial-parallel converts the LVDS data and sends it to Ping-pong buffer. When FIFO address is stable and the signal SLOE# is enabled, SLCS# is asserted, and then FLAG signal which is outputs from CYUSB3014 needs to be monitored. The FLAG signal be configured to show empty or full status. If it is empty status, SLWR# is asserted and the data will is transmitted to 16 bit data bus[10].

2.2 USB3.0 Communication Design

The data transmission of USB3.0 is operated by thread. CYUSB3014 provide, at best, 4 physical hardware threads[10]. According to the system design requirements, CYUSB3014 creates 2 threads: the one is applied to transmitting high speed rate image data is the Super-Speed mode thread, the other is applied to transmitting and receiving command at low speed is the CarKit UART mode thread. A thread includes an endpoint, a socket and a DMA

channel. In a thread, CYUSB3014 connects the USB interface with endpoints and connects the external device with sockets which are registers that pointing to DMA descriptors and storing the address and size of DMA buffer. There is only one DMA channel should be built in the Super-Speed mode thread, because this thread is just used for the external device transmit data to PC. Two DMA channels is built in the CarKit UART mode thread, because this thread needs to transmit and receive command at low speed with PC[10]. In this case, The Super-Speed mode DMA buffer size was set as 128KB and CarKit UART mode DMA buffer size was set as 8KB. Fig.8 shows the DMA channel structure of CYUSB3014.

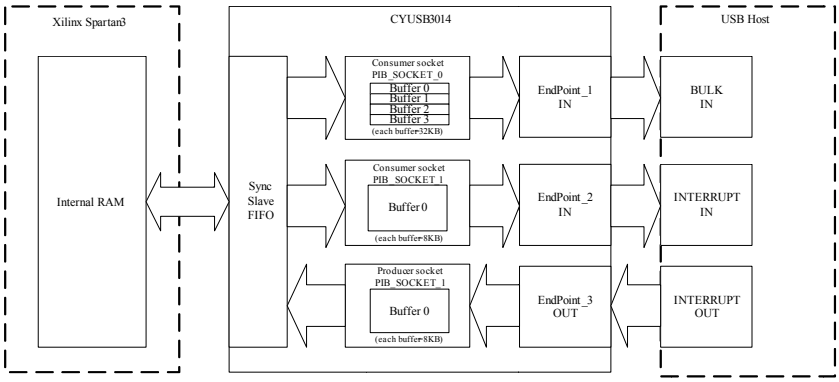

Fig.8 Diagram of DMA channel structure of CYUSB3014

2.3 Circuit Design

The circuit mainly includes FPGA(XC3S400), USB3.0 controller(CYUSB3014), LVDS receiver(DS90LV031), RS-422 transmitter and other peripheral circuits. This circuit adopts 4-layer printed circuit boards. Fig.9 shows the part of design of schematic.

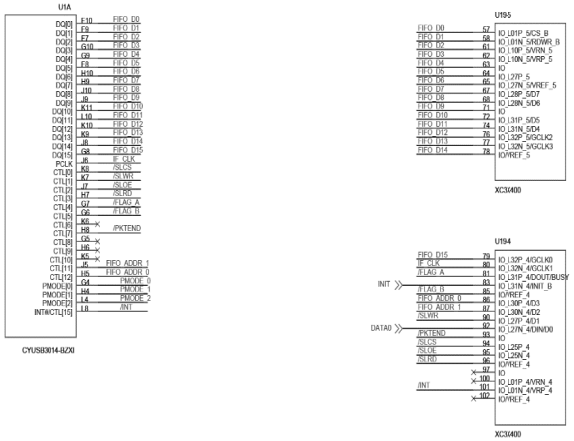

Fig.9 Schematic of the connection between FPGA and CYUSB3014

The appearance of printed circuit board and the PCB are shown in Fig.10 and Fig.11.

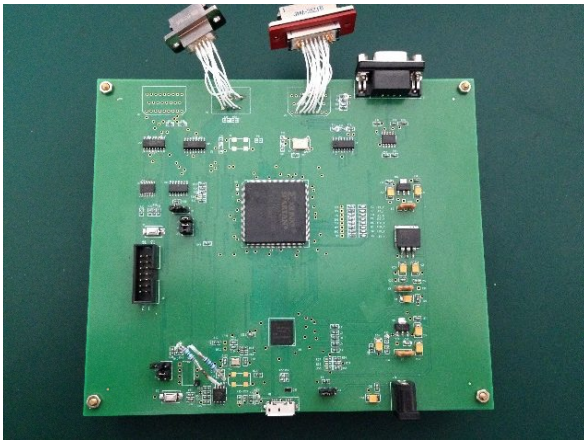

Fig.10 Diagram of Printed circuit board

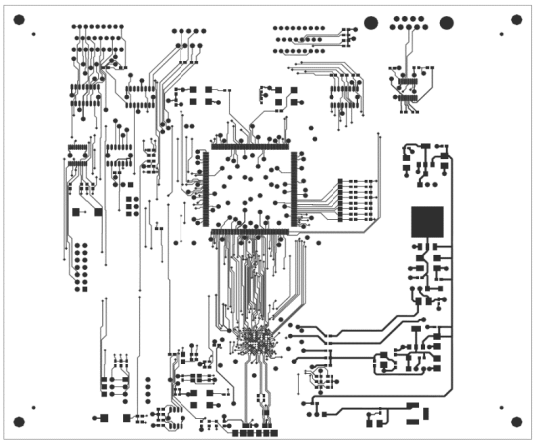

Fig.11 PCB of LVDS to USB3.0 Adapter

The spectrometer ground-testing platform consists of spectrometer, LVDS-USB3.0 adapter and laptop. The operating system of laptop is Windows. Strictly, Windows is not a RTOS. When USB is transmitting data, if more prior events occurs, OS will suspend USB process until CPU returns the control rights[12]. Because of time-sharing strategy and the low priority of USB of OS, the data should be buffered when USB process is paused. According to 128KB buffers of CYUSB3014 and 43Mbps data rate of LVDS, LVDS-USB3.0 adapter can satisfy 23ms pause at most. Using oscilloscope observing the FLAG signal, we found that the longest trigger pulse-width is 12ms when we open webpage and play videos frequently. Using normal camera lens and computer software test the adapter, the imaging result shows that the adapter transmits data steadily in different exposure time. Fig.12 shows the imaging result.

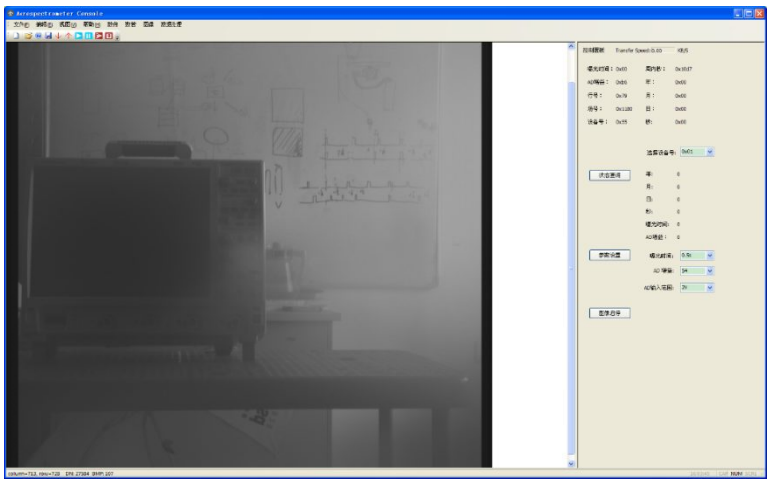

Fig.12 Outfield image of ground-testing platform

With the rapid develop of USB3.0, this article introduces a spectrometer ground-testing platform based on USB3.0, and the platform has been applied to airborne camera. The transmission data rate can reach 2Gbps. Because of the Super-Speed of USB3.0, multi-spectrometer image data can be transmitted simultaneously and higher speed industrial camera can be imaged to PC in real-time.

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