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Electromagnetic interference reduction design of alternating integrator for EAST

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An alternating integrator has been designed for the Experimental Advanced Superconducting Tokamak that is intended for long pulse operation of up to 1000 s. The electromagnetic operating environment for the device is so complex that it could affect the performance of the integrator. The new integrator system is carefully designed and actualized based on specific reduced electromagnetic interference requirements, which were formulated based on consideration of processing of the input signals, the isolation properties, and the circuit board layout and grounding. The developed integrator shows excellent electromagnetic compatibility and low-drift properties. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4962249]

I. INTRODUCTION

Stable and reliable measurement of the device magnetic field is one of the most basic conditions for the operation of tokamaks and plasma control. Magnetic diagnostic systems composed of induction coils and integrators function to measure the magnetic field strength and flux.[1] However, there are two specific difficulties in long-pulse integrator design: (1) as time passes, the integral drift increases and thus prevents the integrator from working with steady-state long pulse plasma; (2) under high-index plasma pulse conditions in the tokamak, the electromagnetic environment is very complex and therefore it is essential to ensure the electromagnetic compatibility (EMC) of the integrator, which is also a prerequisite to maintain the integrator's low-drift property.

To reduce the integration drift, different schemes[2–5] have been used to design integrators for different tokamaks. The integrators designed in this manner have effectively lowered the drift by various degrees.

To date, few published studies have researched the reduced EMI design of these integrators. In the process of design and actualization of these integrators, the authors have found that even if the integrator obtains very good drift results in laboratory tests, the drift properties may degrade during actual tokamak experiments. Worse still, the integrators cannot operate stably. Therefore, this paper describes in-depth research into the EMI reduction of the integrator system.

The electromagnetic environment around EAST is very complex. At the initial stage of the plasma pulse in particular, a very strong electromagnetic field exists that changes dramatically in the space around EAST, and thus may directly interfere with the integrator function. The integrator is an electronic device that is susceptible to interference and it operates in very complex electromagnetic environments in tokamaks. Therefore, it is essential to ensure that the integrator has very good EMC properties because they play a decisive role in the integrator performance.

A prototype of the alternating integrator has been described previously.[6] Also, for practical applications, several different integrator properties were considered, including (1) aspects of systematic grounding and (2) inductive signal transmission through 70 m twisted-pair lines, and the theoretical analysis and testing of these lines.

Section II introduces the integrator system. Section III focuses on reduced EMI measures in the processing of input signals, isolation, and circuit board layout and grounding. Finally, the results of the experiments are discussed in Section IV.

II. INTRODUCTION TO THE INTEGRATOR SYSTEM

The alternating integrator is mainly composed of a field-programmable gate array (FPGA), an integrator with real-time drift compensation, switches, an analog-to-digital converter (ADC), a digital-to-analog converter (DAC), and isolation. The alternating integrator architecture is shown in Fig. 1.

In the new integrator, the integrator with real-time drift compensation[7] is used as one integral cell, while two such integral cells work alternately. The FPGA is used to combine the integral cell outputs to construct a continuous integral of the differential signal.

A transient voltage suppression (TVS) diode is added at the circuit input terminal. To prevent conducted interference from plasma control system and data acquisition system on the integrator, an optical isolation module with very good

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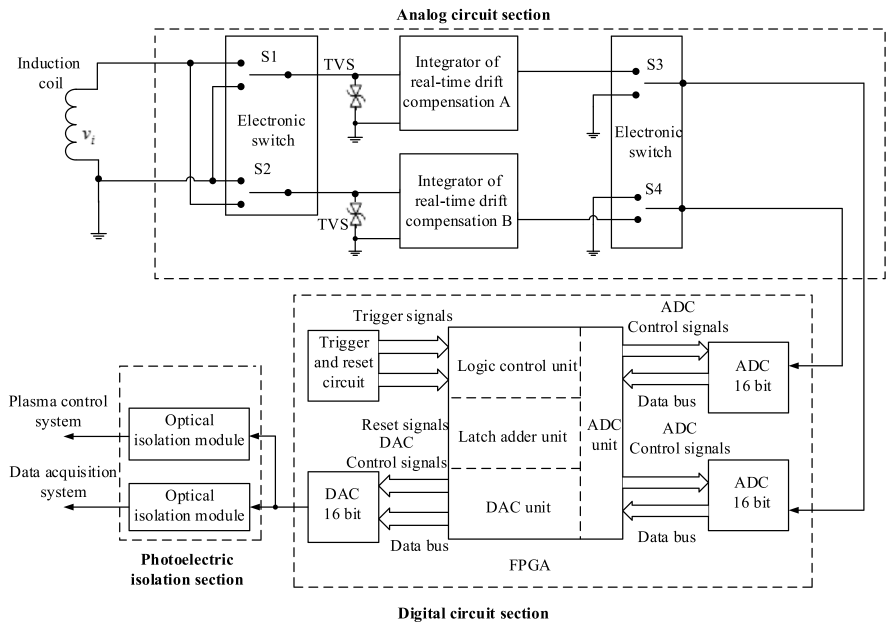

FIG. 1. Alternating integrator system architecture.

linearity is used to isolate the integrator from the following circuit system.

III. EMI REDUCTION DESIGN OF THE SYSTEM

In the overall system, special consideration must be given to EMI reduction design of the integrator. To reinforce its anti-interference abilities, multiple techniques are used to inhibit interference, including input signal processing, isolation, and the circuit board layout and grounding.

A. Input signal processing

To avoid the occurrence of ground loop currents, all inductive signals must be insulated from the vacuum vessel and signals in a state of levitation must be led outside the vacuum vessel. Because the electromagnetic environments surrounding EAST are very complex, the integrator system must be located in a room far away from EAST and 70 m of twisted-pair lines are used to transmit the inductive signals. Therefore, it is essential to analyze and test the effects of use of the twisted-pair lines on the integrator system and consider how to select the grounding method.

As shown in Fig. 2, a Rogowski loop is used as an example that functions to measure the plasma current signals, and a magnetic diagnostics circuit model is set up with a 70 m twisted-pair line.

The simplified model is as shown in Fig. 2(b) and its transfer function is given in Eq. (1),

$$G(s) = -\frac{1}{s}\frac{1}{C(R_R + R_L + R)}. \tag{1}$$

Without the twisted-pair lines, the transfer function can be expressed as follows:

$$G_1(s) = -\frac{1}{s}\frac{1}{C(R_R + R)}. \tag{2}$$

The model parameters are $R_R = 14.227\ \Omega$, $R_L = 5.825\ \Omega$ and $R = 20\ k\Omega$. With R_L and without R_L, Equation (1) can be turned into the following using inverse Laplace transformations:

$$G(t) = -\frac{1}{C(R_R + R_L + R)}u(t) = -49.950\ u(t), \tag{3}$$

$$G_1(t) = -\frac{1}{C(R_R + R)}u(t) = -49.966\ u(t), \tag{4}$$

and the relative error is

$$\xi = \frac{G(t) - G_1(t)}{G_1(t)} = 0.032\%. \tag{5}$$

The error brought by the twisted-pair line is thus around 0.032%. The data collected from the laboratory tests also

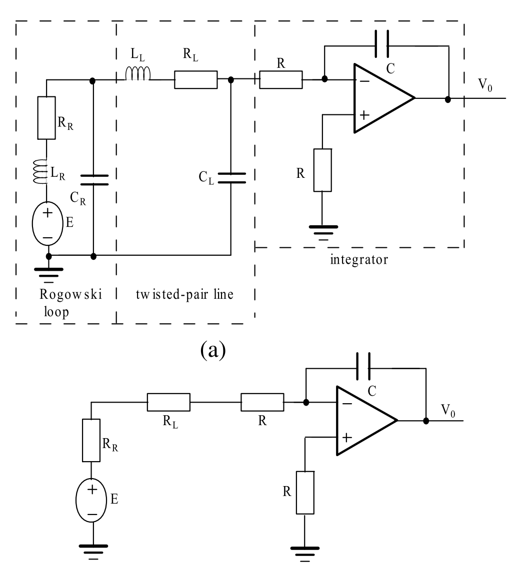

FIG. 2. Circuit model for magnetic diagnostics with 70 m twisted-pair line: (a) model and (b) simplified model.

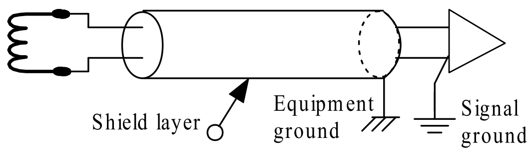

FIG. 3. Grounding method using twisted-pair line.

support the above error analysis, and thus the effects of the 70 m twisted-pair line can be neglected.

As shown in Fig. 3, a single-point grounding is selected in the shield. The two lines of the twisted-pair are connected to the needle and the hole of the Nuclear Instrumentation Module (NIM) connector. The twisted-pair line is connected to the NIM connector case, and is then connected to the equipment ground of the crate through the case.

B. Isolation circuits

In the experiments, the ground of the input terminal of the isolation circuit is tested to see whether or not it requires grounding to the system ground. When the ground of the circuit input is connected to ground, the output signal noise is approximately 10 mV. If it is not connected to ground, then the output signal noise is around 100 mV. The highest noise comes from the 50 Hz signal generated by the power supply. In the real EAST experiments, a series connection is used at the input terminal of the isolation amplifier.

C. EMI reduction design of the integrator circuit board

1. *Circuit board layout*

The integrator circuits can be classified into the three following types. The first type includes those elements and circuits that are easily affected by interference, including the integrator with real-time drift compensation.

These types of circuits all have low voltages and weak signals, and their performance may degrade or even become invalid. The second type includes those circuits that are likely to interfere with the surrounding elements, including the optical isolation circuit. The third type includes those that are likely to severely interfere with the surrounding elements, including the trigger, the reset circuit, the ADC, the DAC, and the FPGA.

The circuit board layout is shown in Fig. 4. Circuits of the first type are located in the lower parts of the board. Circuits of the second type are located on the top right of the board.

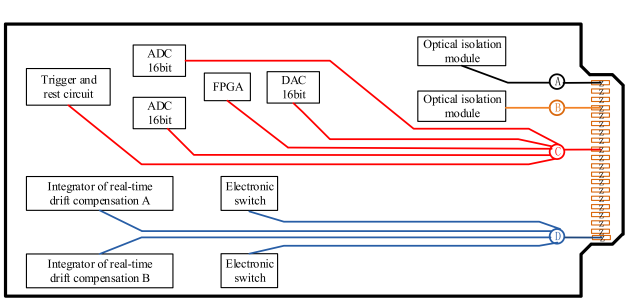

FIG. 4. Layout and wiring of integrator circuit board.

Circuits of the third type are located on the top left of the circuit board.

2. *Treatment of the integrator ground wires*

Voltage differences on the ground wires may lead to severe errors at the output of the integrator, so it is essential to consider their effects. In terms of circuit board design, manual wiring is used. General reduced EMI wiring methods are used to try to increase the ground wire impedance, adopt a ground plane, and select appropriate grounding methods to reduce the effects of these voltage differences.

The power distribution must also be considered. Because the isolation circuit requires two different power supplies and there are two optical isolation sections in the circuit board, the integrator circuit and the front of the isolation circuits share the same power supply, while two power supplies are needed at the ends of the two isolation circuits. Therefore, three linear power supplies are used.

As shown in Fig. 4, appropriate grounding methods are adopted to eliminate effects on the ground wire impedance. In the first circuit type, parallel connections are adopted; the ground voltage of each circuit is only related to its own ground current and ground wire impedance, and is not influenced by other circuits, and this is effective in preventing mutual interferences among the various circuits and the ground loop. Multiple ground lines are required for parallel connections, so the wiring area is enlarged; however, enlargement of the circuit board area is worthwhile when the advantages gained are considered. To prevent inductive coupling among the wires, it is necessary to increase the distances among the various ground wires. We actually ordered a crate after designing the circuit board, so there was no specific board area requirement.

IV. EXPERIMENTAL DATA

In the experiment conducted in the winter of 2016, a new model of integrator system was adopted in the long pulse

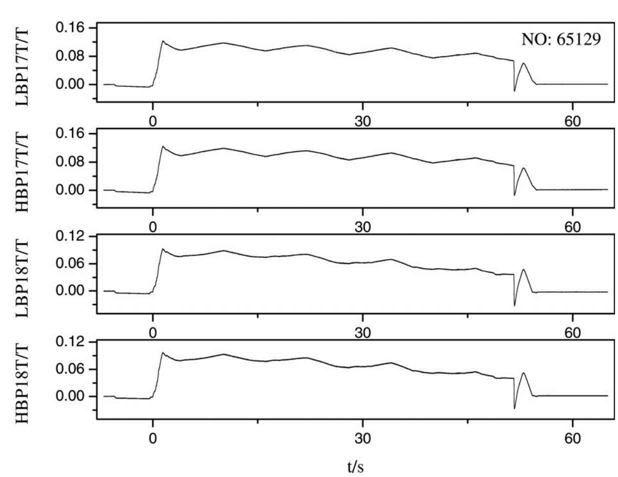

FIG. 5. Experimental data for plasma pulse in EAST (no. 65129). The HBP17T and HBP18T data were acquired using the new alternating integrator system. The LBP17T and LBP18T data were acquired using the previous integrator system.

and its integration time constant is 20 ms and the data of the plasma pulse of 50 s were obtained. From Fig. 5, it can be seen that the drift of the new alternating integrator system within 50 s is less than 10 mV. Because the curve tendencies of the new and previous data are basically consistent, this indicates that the new alternating integrator system can integrate and splice signals well, and that the EMI reduction performance is excellent.

V. CONCLUSION

To design a high-precision and low-drift integrator system, we must systematically adopt suitable measures to design the system structure, the circuit board, grounding, filtering, and other aspects. In the EAST experiments conducted in the spring of 2016, the alternating integrator system showed good coherence and stability, thus proving that its EMI reduction design was reasonable.

ACKNOWLEDGMENTS

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