Fusion Engineering and Design 112 (2016) 57–66

Contents lists available at ScienceDirect

Fusion Engineering and Design

journal homepage: www.elsevier.com/locate/fusengdes

Hardware-in-the-loop simulation of the EAST PF converter for PF control system upgrade

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HIGHLIGHTS

- The hardware in the loop simulation of the EAST PF system is presented.
- The control functions and the protection logic have been tested and verified.
- The major faults could be avoided and commissioning time could be saved on site.

ARTICLE INFO

Article history:
Received 7 February 2016
Received in revised form 23 June 2016
Accepted 27 July 2016
Available online 8 August 2016

Keywords:
Hardware-in-the-loop simulation
Real-time simulation
RT-LAB
EAST PF
Control system

ABSTRACT

The EAST poloidal field (PF) control system was upgraded in 2015 and the new system has been in use for the 2015 EAST campaign. This paper presents the implementation of a hardware-in-the-loop (HIL) simulation platform of the EAST PF converter system based on the RT-LAB simulation environment, which was used to improve and evaluate the performance of the real controller. The EAST PF power supply system and its operational modes are presented in this paper. The experiments on HIL simulation platform show that the control algorithms and the over current protection of the controller meet the design requirements well. In addition, the effectiveness of the designed control system has been verified by actual application during the EAST campaign at 2015 for six months.

1. Introduction

The Experiment Advanced Superconducting Tokamak (EAST) is a non-circular advanced steady-state experimental device located at the Institute of Plasma Physics (ASIPP), Chinese Academy of Sciences [1–3]. The EAST PF power supply system consists of AC/DC converters, bi-direction external bypass, Switching Network Units (SNU), and a Quench Protection (QP) circuits [4]. Each converter operates in four quadrants to provide the slow ramp up and control of current necessary to produce the requested plasma shape and position [5].

The EAST PF power supply system was designed more than ten years ago and has been in service since then. Because of technological and cost limitations which was existed 10 years ago, the accuracy and linearity of the original power supply control system were not very good. The performance of PF converter system could not meet the plasma control requirements or improvements that were necessary in the plasma operating mode. It became necessary to upgrade the control system of the PF power supply system. Considering the complexity and variability of the control logic, it was decided to fully test the new control system before implementing it on the real main circuit so that major problems and faults can be avoided. In this paper, the HIL technology is applied to improve and verify the control system design and reduce the time for system commissioning on site, specially to test four quadrants control logic, voltage response time and over current detection function and protection logic.

The paper is organized as follows: Section 2 presents a brief analysis of the EAST PF converter system and its control system. The HIL simulation is presented in Section 3. In this part, the details in creating the real-time simulation model of main circuit are included and the monitoring interface designed by LabVIEW is presented. Section 4 shows the simulated results obtained with HIL simulation and the actual experiments on the EAST PF converter system are carried out to verify the effectiveness of the designed controller and the validity of the HIL simulation. The conclusions are drawn in Section 5.

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http://dx.doi.org/10.1016/j.fusengdes.2016.07.020
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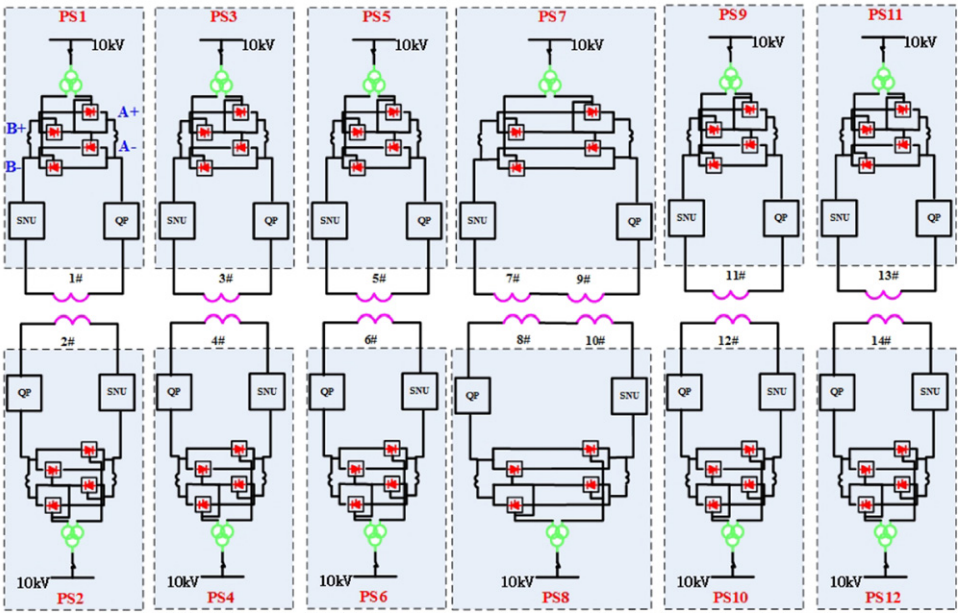

Fig. 1. The architecture of the EAST PF power supply system.

2. The EAST PF converter system

There are 12 PF power supplies that feed 14 PF coils (including the central solenoid coils). The power supplies have voltage ratings range from ±0.35 kV to ±1.1 kV with a common current rating of ±15 kA. The architecture of the EAST PF power supply system is shown in Fig. 1.

2.1. The operational modes of the EAST PF converter system

The operational modes of the EAST PF converters comprises of parallel mode, single bridge mode and circulating mode. The circulating mode facilitates smooth current zero crossing and avoids open circuit and high voltage on the coil. The PF converter system operates using parallel mode when a large load current is required. In this case, two six-pulse bridges oriented in the same direction and work together to supply the current to the load and produce a twelve-pulse output voltage. Single bridge mode is used during the transition period between circulating mode and parallel mode. Operational modes are switched according to the load current value as explained in Table 1. The A+, A−, B+ and B− are the six-pulse converters, as shown in Fig. 1.

2.2. The control system of the EAST PF converter system

Fig. 2 shows the architecture of the EAST PF control system. A Master Controller (MRC) receives reference voltage signals from the Plasma Control System (PCS) and dispatches it to the local controllers (LCC). Each LCC controls two set of converter units. The LCC calculates the firing angle according to the reference signals from MRC and sends it to the alpha controller. The alpha controller sends the fiber optic signal at the appropriate time to the pulse generator.

Table 1
Operational mode.

Id/Imax	<−15%	−15%~−10%	−10%~10%	10%~15%	>15%
Bridge Operational mode	A− B− Parallel	B− Single	A+ B− Circulating	A+ Single	A+ B+ Parallel

The pulse generator transforms the fiber optic signal into an electrical signal to trigger the thyristors. The three operational modes and the switching between modes are controlled by LCC while the coil current closed loop control is realized in the PCS. The hardware configuration of the LCC is given in Fig. 3 which is composed of CPU board, alpha controllers, AI board and DI/DO board and the relative interface, based on CompactPCI bus [6,7].

2.3. The design requirements for the EAST PF converter system

According to the plasma control requirements, the design requirements for the EAST PF converter system are as follows:

(1) The circulating current value should be 2 ± 0.5 kA;
(2) |(ID1-ID2)/ID1|<10% in parallel mode (If Id > 0, ID1, ID2 represent the IA+ and IB+, else if Id < 0, ID1, ID2 represent the IA− and IB− respectively);
(3) The PF converter shall provide the symmetrical voltage response not more than 20 ms for full scale change.

Due to the complexity of the control system and the high power rating of the EAST PF converter system, any misoperation of the controller might damage the equipment. By connecting the real controller to high-fidelity simulation of the main circuit, the HIL

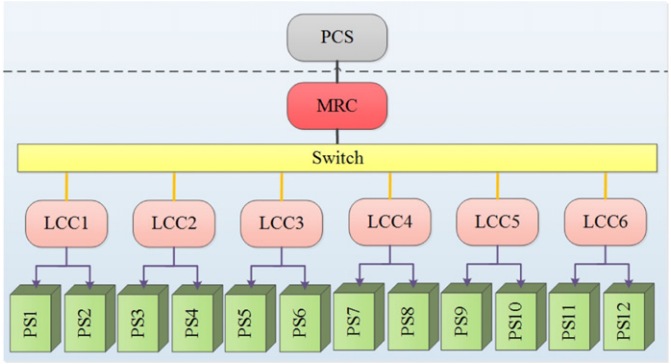

Fig. 2. The architecture of the EAST PF control system.

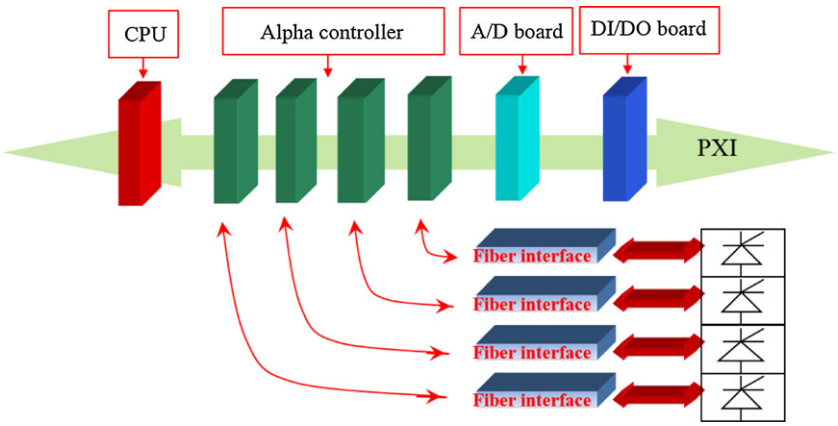

Fig. 3. Hardware configuration of LCC.

simulation is a very effective and advantageous method to test the real controller under various simulated conditions.

3. The HIL simulation with RT-LAB

3.1. The RT-LAB simulator

Real-Time Laboratory (RT-LAB) developed by Opal-RT Technologies is widely applied in HIL simulation for system integration, design, verification, test and so on [8–13]. RT-LAB is a real-time simulation platform, which can shorten development time and is very cost effective [14]. The reliability of the RT-LAB simulator has been proved in many fields, such as the fuel cell hybrid vehicle [8], FPGA [9], power electronics systems [10], metro vehicle linear induction motor driving system [12], etc. RT-LAB allows the user to readily convert simulation models to real-time simulations [15]. It also supports many commercially available I/O cards and can be easily interfaced with various simulation tools like CarSim, LabView and Altia [16]. The hardware configuration of RT-LAB simulator shown as Table 2.

3.2. The HIL simulation of the EAST PF converter system

HIL simulation is a dynamic test technique that provides a simulated environment for the real controller (hardware) under test, simulating the parts of the system that are not physically present with real-time plant model (software) [17–19]. Fig. 4 shows the HIL simulation platform topology of the EAST PF converter system. The software realization includes the simulation of the main circuit with RT-LAB and the monitoring interface with LabVIEW.

Table 2
The hardware configuration of RT-LAB simulator.

Items	Quantity	Description
Operating system	1	QNX v6.5.0
Chassis type	1	OP5600 Chassis
CPU	2	Intel Xeon Six-Core 3.33 GHz 12M Cache
Memory	4	1 GB
OP5330	2	16 Aout
OP5353	2	32 Din
OP5354	2	32 Dout

3.3. The RT-LAB simulation and the monitoring interface

3.3.1. The RT-LAB simulation of the EAST PF converter system

The command station will supervise the target PC by TCP/IP while the main circuit is executed. The main circuit is created in Simulink and modified based on RT-LAB model libraries and subsystems separating rules. The RT-LAB simulation model of the EAST PF main circuit is shown as Fig. 5. The main circuit interacting with the real controller via I/O in RT-LAB simulator. The synchronizing signals and the measured signals must be linked to the card driver procedure in Aout32 and Din32 module in Fig. 5. All the signals exchanged between the real-time plant model and the real controller are at low power levels typically within a range of +/−5 ~ +/−10 V which can be easily implemented by A/D converters or D/A converters with acceptable accuracy [20].

3.3.2. The monitoring interface

In order to observe the key data such as firing pulses, currents and voltages of converter, the monitoring interface is designed in LabVIEW and loaded in RT-LAB by TEST derive. The monitoring interface is indicated in Fig. 6. Part A is a parameter setting area and

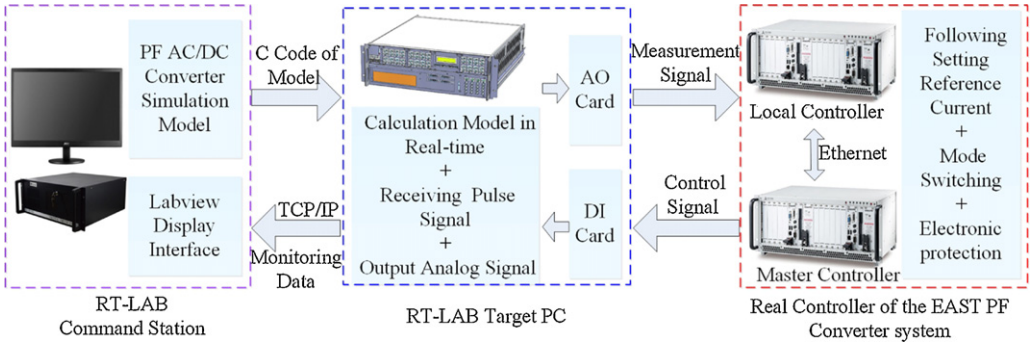

Fig. 4. The HIL simulation platform topology of the EAST PF converter system.

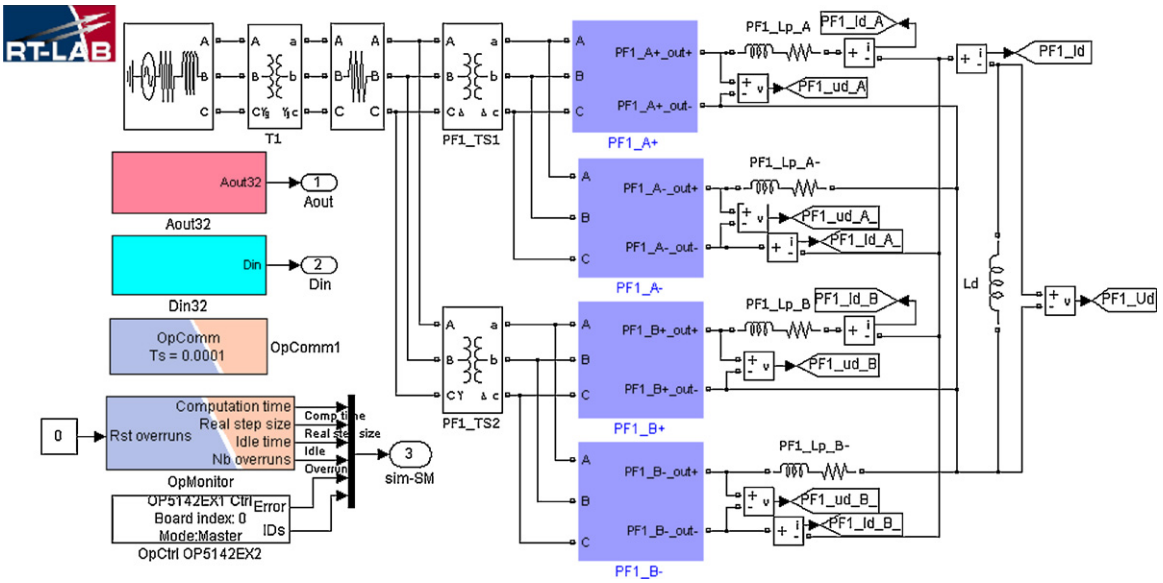

Fig. 5. The RT-LAB simulation model of the EAST PF main circuit.

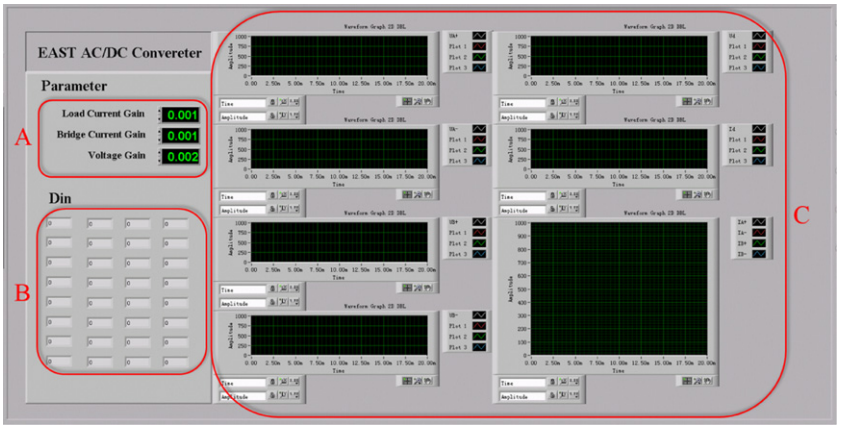

Fig. 6. Monitoring interface with Labview.

part B is used to display whether the trigger pulse sent or not. The number will be 1 if the pulse is transmitted, otherwise the number will be 0. The current and voltage are displayed in part C.

4. HIL simulation and experimental results

The following sections show the experimental results of different operational modes and the over current protection. The HIL simulation experiments are carried on one PF converter at a time. The control logic of each PF converter is the same except the parameters, therefore the experiments of only one PF converter will be provided. I_{ref} and I_d are the reference currents and load current. The IA+, IA−, IB+, IB− are the bridge currents. I_{cref} and I_c are the reference circulating current and actual circulating current respectively. VI is the secondary winding voltage. α_1, α_2 are the control angles for converter1 and converter2.

4.1. The circulating mode

Figs. 7 and 8 show the control block diagrams and the current paths of circulating mode respectively. The circulating current is defined as the constant value of I_{cref} which is 2000 A in the EAST PF

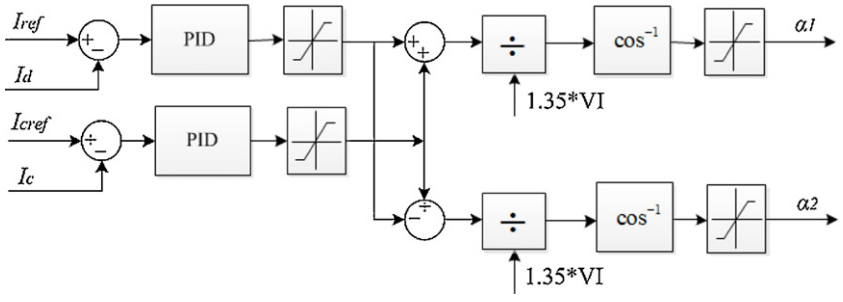

Fig. 7. The control block diagram of circulating mode.

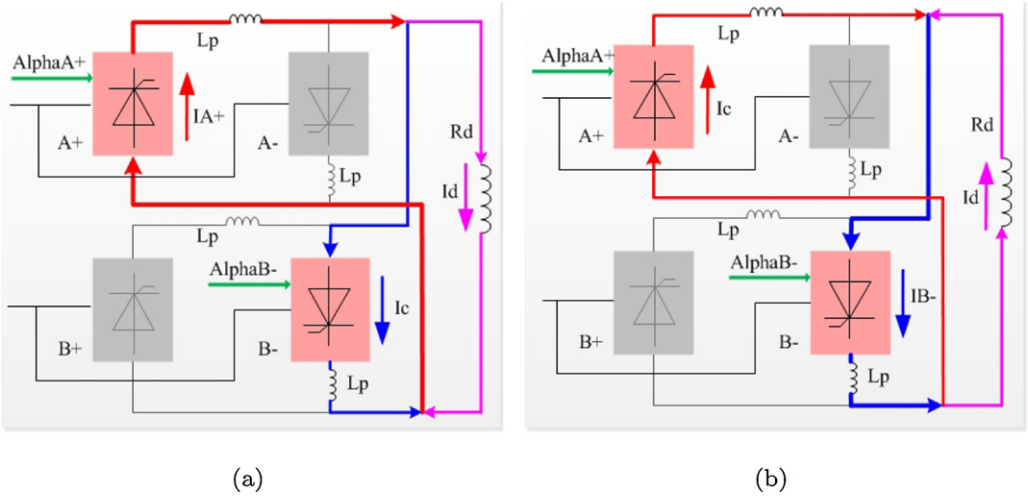

Fig. 8. Current paths in the case of circulating mode. (a) When Id is positive. (b)When Id is negative.

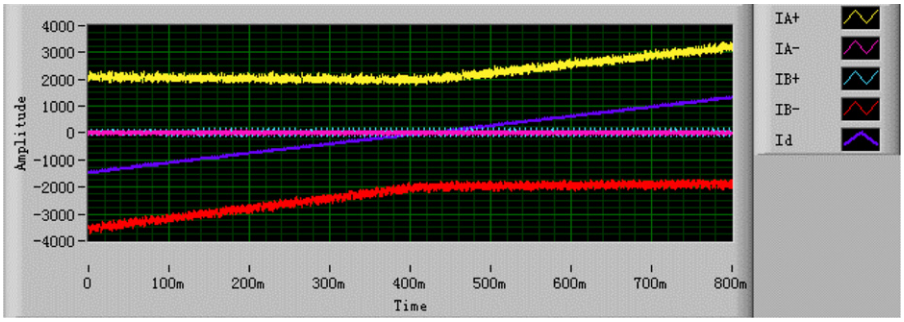

Fig. 9. The circulating mode with HIL simulation.

converter system. The bridge A+ supplies the I_c when the I_d is positive [Fig. 8(a)], otherwise the bridge B− supply the I_c [Fig. 8(b)]. The I_d is obtained by the sum of IA+ and IB−. Fig. 9 shows the circulating mode with HIL simulation. The circulating currents are −2000 A, +2000 A when the I_d are negative and positive, and the I_d follows the I_{ref}, which illustrate that the circulation control logic, hence, satisfying the design.

4.2. The single bridge mode

Figs. 10 and 11 show the control block diagrams and the current paths of single bridge mode. There are two operating bridges before the PF converter enters into single converter operation. Hence, according to the positive and the negative current, the gate pulses of the bridge which does not feed the load current will be suppressed. The bridge A+ feed the I_d when the I_d is positive [Fig. 11(a)] otherwise bridge B− feed the I_d [Fig. 11(b)]. Fig. 12 shows the single bridge mode with HIL simulation. Fig. 12(a) and (b) shows the bridge A+, bridge B− feed the I_d respectively, which prove that the single bridge control logic is correct.

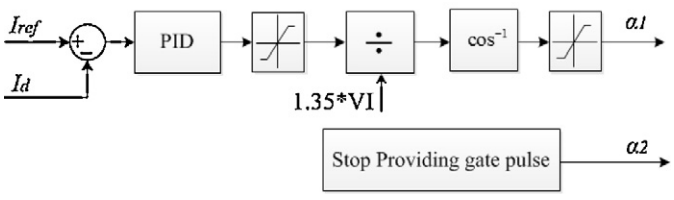

Fig. 10. The control block diagram of single bridge mode.

4.3. The parallel mode

Figs. 13 and 14 show the control block diagrams and the current paths of parallel mode. In parallel mode, two parallel bridges feed the I_d on average. Thus, the current of one bridge I1 is following the other bridge current I2 while the I_d is following the reference current. Bridge A+ B+ work in parallel to feed the I_d when the I_d in positive [Fig. 14(a)] otherwise the bridge A− B− operate in parallel [Fig. 14(b)]. Fig. 15 shows the parallel mode with HIL simulation. Fig. 15(a) and (b) show the I_d is supplied by IA+ IB+ and IA− IB− respectively which shows that the parallel control logic is correct.

4.4. Four quadrant operation

Figs. 16 and 17 show the four quadrant operation with HIL simulation and the actual operating of the EAST PF convert system7. The ps7idccu1c1, ps7idccu1c2, ps7idccu2c1, ps7idccu2c2 are the currents of the bridge A+, A−, B+, B− respectively. The ps7idc1 is the load current. The simulation results in Fig. 16 agreed with the actual operation results in Fig. 17, which illustrated the accuracy of the controller in the EAST PF converter system.

4.5. Voltage response time

Figs. 18 and 19 show that the voltage response time with HIL simulation and the actual operating of the EAST PF convert system7 are both 15ms. The HIL simulation is consist with the actual operating and the voltage response time satisfy the requirement.

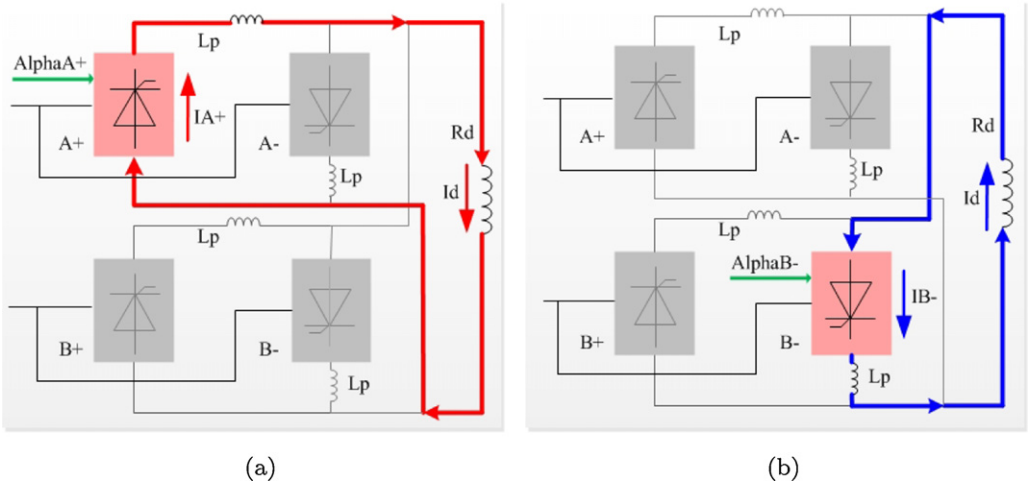

Fig. 11. Current paths in case of single bridge mode. (a) When Id is positive. (b) When Id is negative.

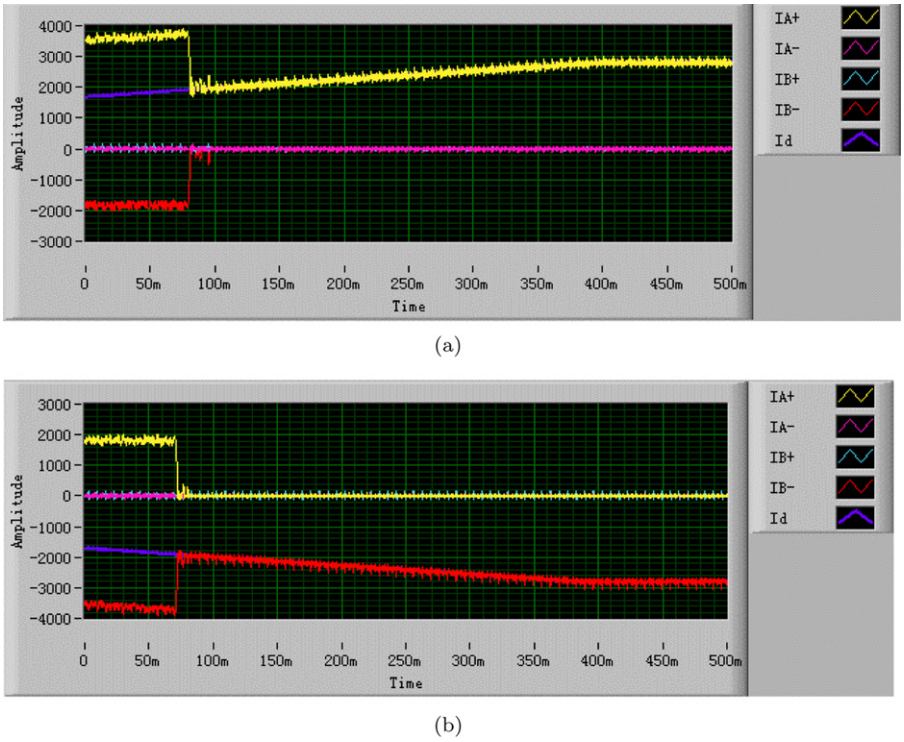

Fig. 12. Single bridge mode with HIL simulation. (a) When Id is positive. (b) When Id is negative.

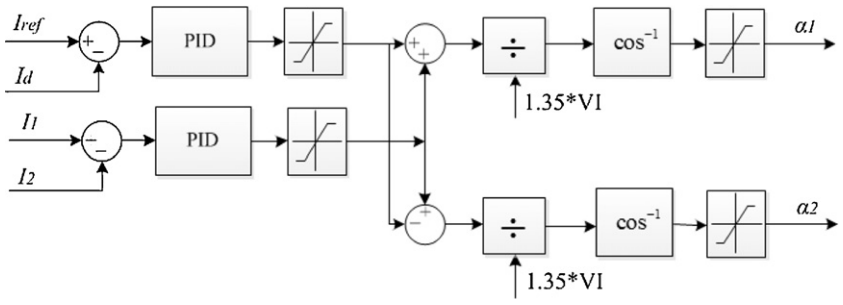

Fig. 13. The control block diagram of parallel mode.

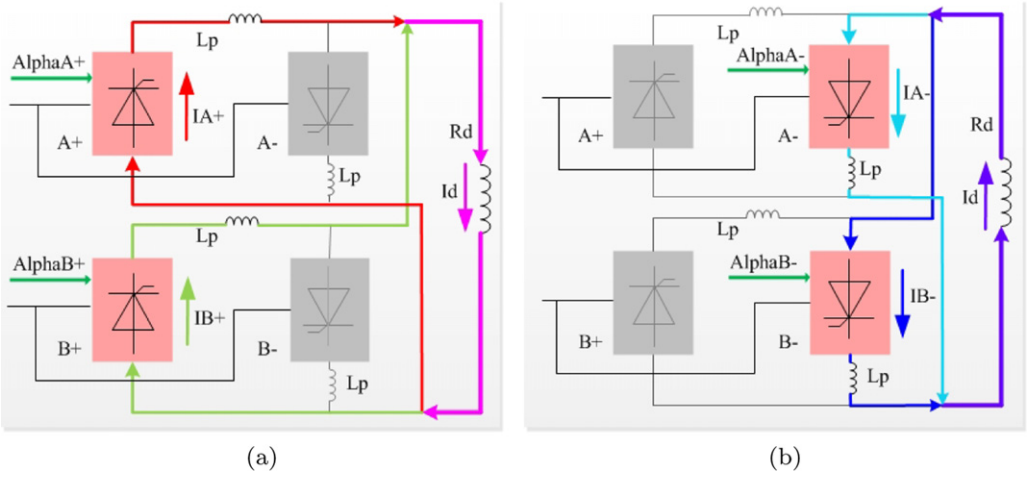

Fig. 14. Current paths in the case of parallel mode. (a) When Id is positive. (b) When Id is negative.

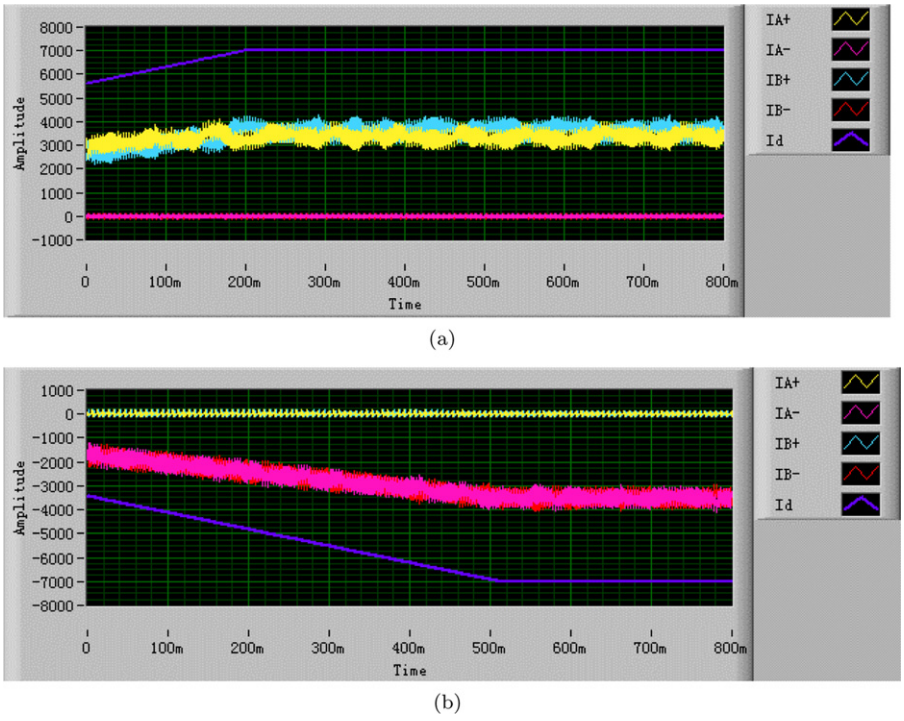

Fig. 15. Parallel mode with HIL simulation. (a) When Id is positive. (b) When Id is negative.

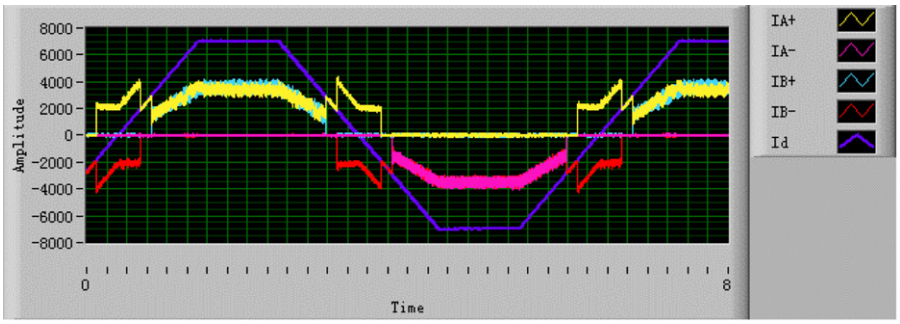

Fig. 16. Four quadrant operation with HIL simulation.

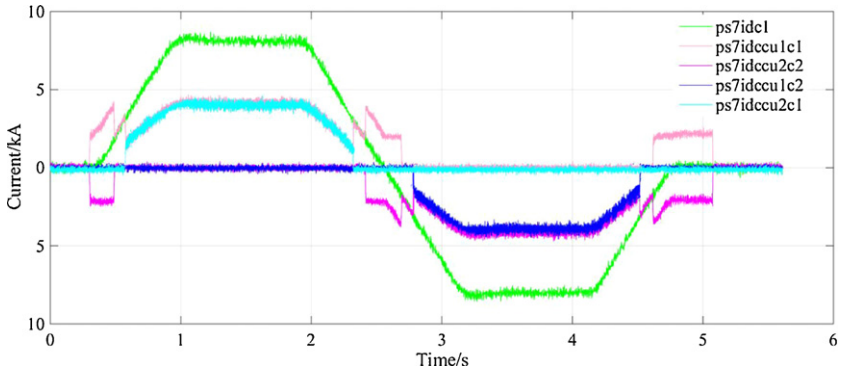

Fig. 17. Four quadrant operation of the EAST PF converter system.

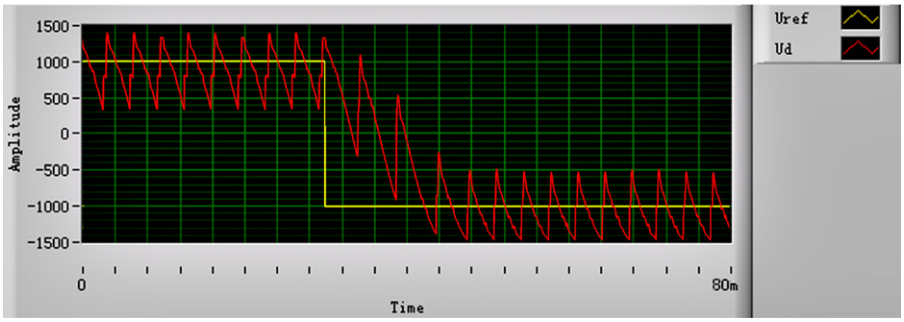

Fig. 18. Voltage response time with HIL simulation.

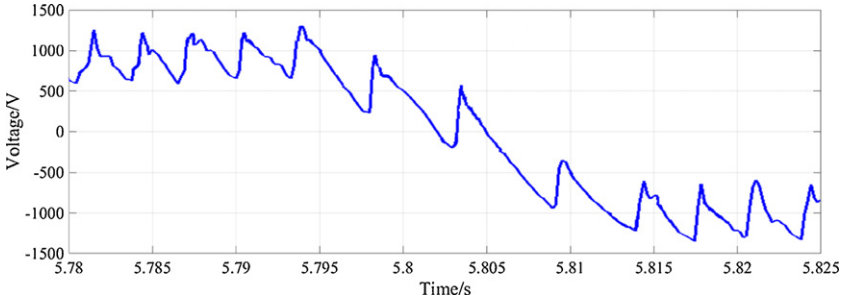

Fig. 19. Voltage response time with the actual operating.

4.6. The comparison between HIL simulation and the actual operating

Table 3 shows the comparison between HIL simulation and the actual operation. The parameters of circulating current and the |(ID1-ID2)/ID1|<10% in parallel mode are calculated based on the experiments of four quadrant operation [Figs. 16 and 17]. ID1 and ID2 represent IA+(IA−), IB+(IB−) respectively. The HIL simulation experiment results agreed with actual operating and meet the requirements well, which illustrate that the HIL simulation is a very effective tool to validate the effectiveness of the controller. The error between the HIL simulation and the actual operating could be the measuring error.

Table 3
The comparison between HIL simulation and the actual operating.

	Design	HIL simulation	Actual operating
Circulating current	2 ± 0.5 kA	2 ± 0.29 kA	2 ± 0.35 kA
|(ID1-ID2)/ID1|	<10%	7.7%	8.6%
Voltage response time	<20 ms	15 ms	15 ms

4.7. The over current protection

The over current protection plays a vital role in the EAST PF converter system for safe operation. Many failures for the power supplies, such as the shortage of the load, thyristor failure, etc, lead to over current scenario. Any failure to handle a fault properly may lead to equipment damage. As an advanced design/test method, the HIL test allows the prototype of a novel apparatus to be investigated under a wide range of realistic conditions repeatedly, safely and economically.

The over current protect logic consists of instantaneous regulating the gate pulses and firing the bypass thyristors with a train of pulses. The converter bridges are inverted first. In order to avoid inversion failure and fault propagation, suppression of the gate pulses will only take place after the inversion.

Figs. 20 and 21 show the HIL simulation experiment results and the actual application of over current protection on the EAST PF converter system5. The PS5IDC1, ps5idc2 and PS5IDC3 are the load currents. The ps5vdc is the load voltage and the refv5 is the load voltage reference sent by PCS. Fig. 20 is consistent with Fig. 21, both of which illustrate that the converter system exit safely under over current situation.

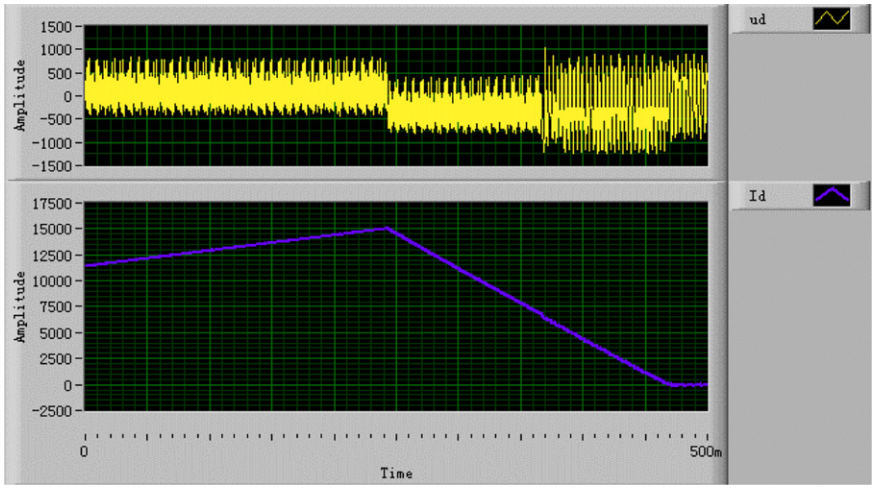

Fig. 20. Over-current protection with HIL simulation.

Fig. 21. Over-current protection of the EAST PF converter system.

5. Conclusion

In this paper, the HIL simulation of the EAST PF converter system is implemented based on RT-LAB simulation environment which is used to evaluate and improved the design of the new control system before installed on site. The control system is implemented in hardware and the main circuit is built in RT-LAB with simulation. The results of HIL tests and the application in the EAST PF converter system demonstrate that HIL simulation is a very effective tool to validate the effectiveness of the real controller under various realistic conditions and the designed controller meet the requirements well. The time needed for system integration and commissioning

on site is saved. The HIL simulation approach ensured that the PF control system upgrade is on schedule and the new control system is placed in service in the EAST Tokamak on time at the end of 2015.

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