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Modulation of interfacial and electrical properties of HfGdO/GaAs gate stacks by ammonium sulfide passivation and rapid thermal annealing

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A B S T R A C T

In this work, the interface chemistry and the reduction of GaAs surface species by using $(NH_4)_2S$ solution prior to Gd-doped HfO_2 (HGO) thin film deposition and the removal of Ga Oxides and elemental As by rapid thermal annealing (RTA) have been investigated by X-ray photoelectron spectroscopy (XPS). Additionally, the effect of the surface passivation and rapid thermal annealing on the electrical properties of MOS capacitors based on sputtering-derived HGO as gate dielectric on GaAs substrate has been detected by means of capacitance-voltage (*C-V*) and leakage current density-voltage (*J-V*) measurements. Based on electrical analysis, it can be noted that the constantly improvement of electrical properties, such as the decreases of flat band voltage (V_{fb}), hysteresis (ΔV_{fb}), oxide charge density (O_{ox}), border trapped oxide charge density (N_{bt}) and leakage current density, have been observed. Especially, the dielectric constant of 16.72, flat band voltage V_{fb} of 1.19 V, hysteresis ΔV_{fb} of 0.04 V, leakage current density of 1.54×10^{-5} A/cm^2 at bias voltage of 1 V, total positive charge density and border trap charge density of 6.09×10^{12} cm^{-2} and 2.54×10^{11} cm^{-2}, respectively render 600 °C-annealed HGO thin films, potential high-k gate dielectrics in future CMOS devices.

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1. Introduction

III-V semiconductors and high dielectric constant (k) materials have become an imperative for down scaling of metal-oxide-semiconductor (MOS) based devices. III-V semiconductor GaAs has potential advantage over Si-based MOS devices due to its high breakdown field, direct energy band gap and high electron mobility. Those merits render GaAs to supersede silicon as the channel material and thus extends Moore's law on si-based MOS scaling beyond the 22 nm node [1–3]. Before this potential is unearthed, a number of challenges need to be overcome. Compared to the MOS interface between SiO_2 and Si, the absence of a reliable dielectric on GaAs retards the development of GaAs-based MOS structure. The conventional SiO_2-based gate dielectrics in MOS devices have been outdated because its thickness cannot reach the limit below 1.0 nm. Fortunately, recent progress indicates that high-k dielectrics are the suitable alternatives. However, a poor dielectric interface due to native oxide is likely to cause the Fermi-level pinning at the midgap, which prevents the formation of accumulation or inversion layers [4]. As a result, it is critical for removing the surface species to unpin the Fermi level. An effective surface passivation is of great practical importance. As a solution, the use of an interface passivation layer between GaAs substrate and high-k gate dielectric such as AlON [5], AlN [6], Si [7], ZnO [8] improve the device performance but at the cost of the extra process complexity. However, the sulfur-based chemicals such as ammonium sulphide $(NH_4)_2S$ solution have been proved to be a moderate etchant to GaAs [9]. It can remove the native oxides on GaAs and further passivate the surface dangling bonds of GaAs to prevent from oxidizing. Among numerous high-k gate dielectric materials, hafnium oxide thin films have been investigated actively due to its promising application in metal oxide semiconductor field effect transistor, capacitor dielectric of dynamic random access memory, optical devices as well as thermal protective coating [10–13]. However, the low crystallization temperature and moderate

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dielectric constants restrict the further development of HfO_2-based MOS devices [14]. A feasible way to enhance the performance of the HfO_2 films is use binary oxides such as Al-HfO_x [15], Y-HfO_x [16], La-HfO_x [17], Gd-HfO_x [18]. Previous investigations have confirmed that rare earth element Gd could be doped into HfO_2 to change electronic structure [19], enhance crystallization temperature [20], increase dielectric constant [21] and conduction band offset [22]. Up until now, there is almost no related study on integrating HGO thin films into GaAs MOSFET devices, especially, sputtering-derived HGO gate dielectric on $(NH_4)_2S$-treated GaAs substrate.

In current work, Gd element was selected as an incorporation added in HfO_2 film to improve interfacial and electrical properties. Additionally, more attention have been paid to the evolutions of the interfacial chemical composition and electrical properties in Al/HGO/GaAs MOS structure as a function of the S-passivation process and rapid thermal annealing temperature by means of characterization from X-ray photoelectron spectroscopy(XPS), high frequency capacitance-voltage (*C-V*) and current density voltage (*J-V*) measurements.

2. Experimental

Commercially available n-type GaAs wafers with a resistivity of (1.2–1.6) $\times$ 10^{-3} Ω.cm were chosen as the substrates. The GaAs wafers are obtained from the Hefei kejing materials technology limited company. Prior to HGO thin films deposition, the GaAs substrates were ultrasonically cleaned by acetone, ethanol, methanol, isopropanol for 5 min at room temperature to remove organic and metallic impurities on the wafers (denoted as organic cleaning), immersed in a diluted HBr solution for 5min to remove native oxides (denoted as acid cleaning), and soaked in $(NH_4)_2S$ for 20 min at 50 °C to passivate the GaAs (denoted S-passivation) and dried by high purity nitrogen. After cleaning, the GaAs substrates were loaded into the vacuum chamber of a magnetron sputtering equipment (JGP-DZS, Chinese Academy of Sciences, Shenyang Scientific Instrument Co., Ltd.) immediately. Before deposition, the vacuum chamber was evacuated to 5.0 $\times$ 10^{-4} Pa. The radio frequency reactive sputtering of HGO (atomic ratio of Hf:Gd = 9:1) ceramic target was employed to deposit HGO thin films on the GaAs in Ar ambient with the flow rates of 20 SCCM (SCCM denotes cubic centimeter per minute at STP). The RF power, working pressure, and deposition temperature were fixed at 60 W, 0.6 Pa, and room temperature, respectively. In order to observe the effect of S-passivation on the interface chemistry of GaAs wafers, three sets of samples (S1, S2, S3) have been prepared, which are assigned as organic cleaning, organic cleaning and acid cleaning, organic cleaning and acid cleaning and S-passivation, respectively. After that, ex situ post deposition annealing (PDA) was conducted under N_2 ambient condition for S3 sample at the temperature of 300, 400, 500 and 600 °C, which marked as PDA@300 °C, PDA@400 °C, PDA@500 °C, PDA@600 °C, respectively. Fig. 1 shows the details of the experimental procedure for GaAs wafer cleaning, HGO films deposition and CMOS device fabrication. About 8 nm thick HGO films measured by spectroscopy ellipsometer (SC630, SANCO co, Shanghai) were prepared for XPS measurement to probe the interfacial chemical composition and chemical bonding state between GaAs substrate and HGO thin film. The XPS measurements were equipped with an Al Kα radiation source (1486.6 eV) and all the collected data were calibrated using the binding energy of C1s peak (284.8 eV). In order to explore the electrical properties, a series of Al/HfGdO/n-GaAs/Al MOS capacitors were fabricated by sputtering a Al-top electrode with the area of 7.065 $\times$ 10^{-8} m^2 through a shadow mask and Al was also deposited as the back electrode to decrease the contact resistance. The high-frequency (1 MHZ) *C*–*V* curves and leakage current characteristics *J*-*V* were performed using a semiconductor device analyzer (Agilent B1500A) and Cascade Probe Station. The MOS capacitors were firstly placed in probe station, and then move the probe to the Al-top electrode, cover the dark box and close the floodlight. Before test, all the electrical tests were required to short circuit and open circuit calibration using semiconductor device analyzer.

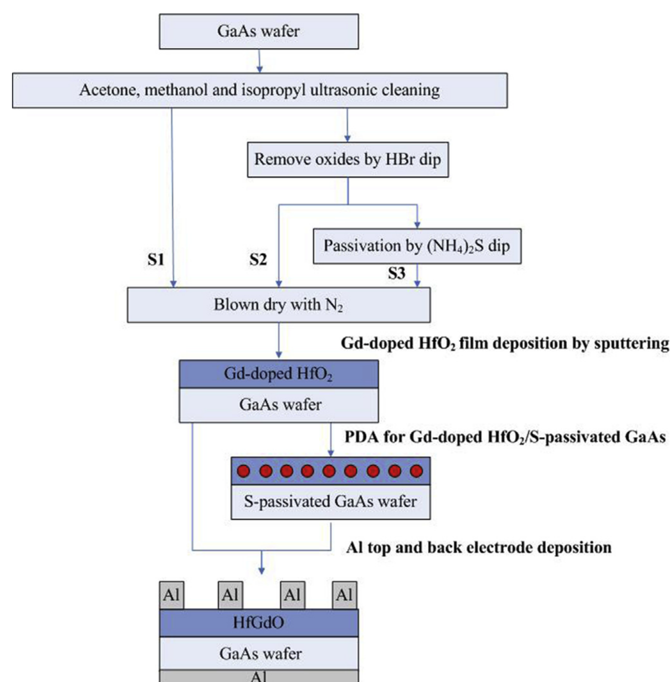

Fig. 1. The schematic flow chart of the HGO thin film synthesis by magnetron sputtering method.

3. Results and discussion

3.1. XPS analysis of S-passivation process

The effect of S-passivation process on the interfacial chemical composition of HfGdO film has been investigated using XPS. Fig. 2 exhibits the survey spectrum of sample S1, S2, and S3 at the

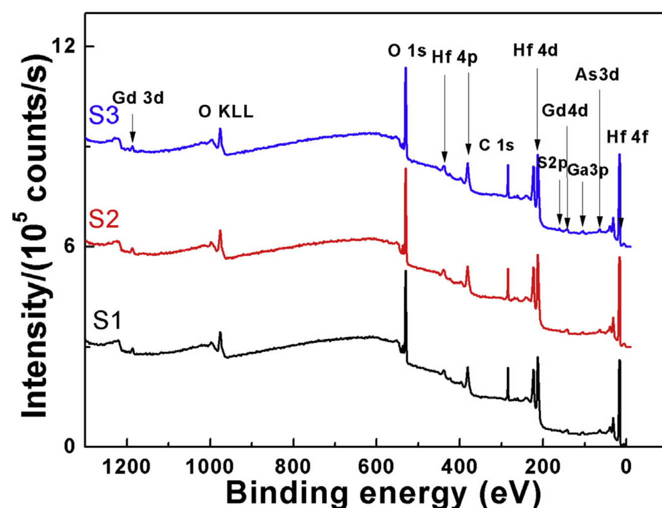

Fig. 2. Core level XPS survey spectra of S1, S2, S3.

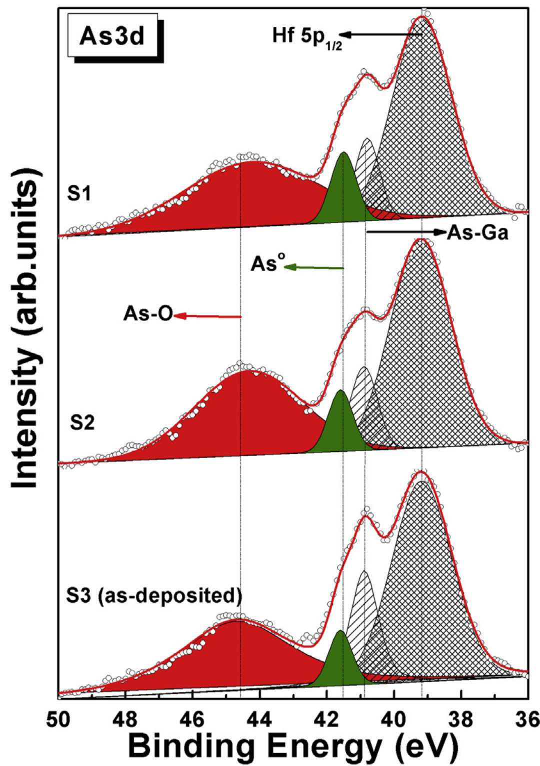

Fig. 3. As 3d core-level XPS spectra of S1, S2, S3.

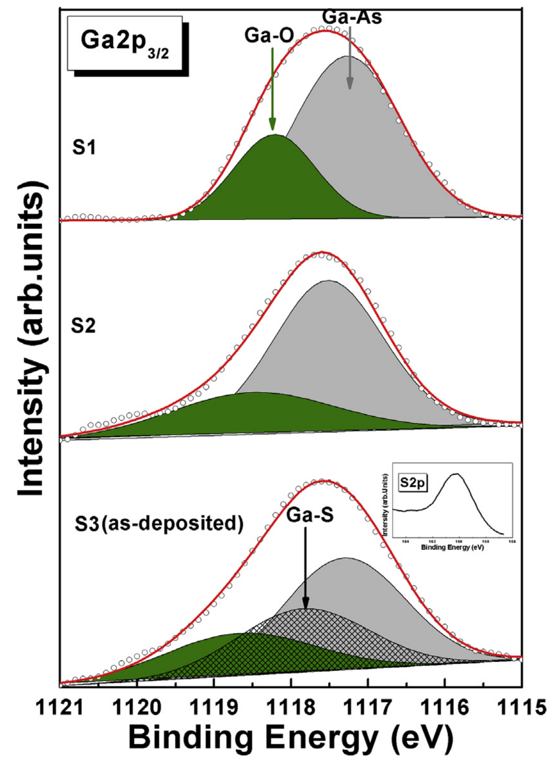

Fig. 4. Ga 2p $_{3/2}$ core-level XPS spectra of S1, S2, S3.

bindingenergy range from 0 to 1300 eV. Only element Hf, Gd, O, As, Ga, and C introduced from thin film disposition process or air contamination during measurement have been detected, indicating that the films were escaped from contamination and also confirming that the element Gd successfully incorporated into HfO_2 gate dielectric. In addition, the appearance of S 2p in the sample S3, indicating that the S atom has been doped into GaAs interface. Fig. 3 presents As 3d core level spectra of the sample S1, S2, S3. As 3d spectra of all samples could be deconvoluted into four subpeaks, corresponding to Hf $5p_{1/2}$ (~39.16 eV), As–Ga (~40.87 eV), elemental arsenic As^o (~41.51 eV) and As–O (~44.58eV), respectively. Similar XPS peak fits with As^o, As–O and Hf $5p_{1/2}$ have been reported previously for ALD-derived HfAlO on GaAs [23] and PLD-derived HfO_xN on GaAs [24]. The intensity of Hf $5p_{1/2}$ peak is observed to be obviously higher than other bonds, which can be due to the substrate being covered by a layer of HGO film that attenuates the photoelectron signals. It can be observed that after acid cleaning and S-passivation, the element As^o component is apparently reduced while the As–O (mixture of As^{3+} and As^{5+}) component almost remain unchanged. Meanwhile, all samples are almost no peak position deviation. It is reported that interface species element As^o is unstable on heated GaAs surface and have a tendency to toward evaporation [23]. The decrease in As^o component may be due to the higher soak temperature in $(NH_4)_2S$ solution causing a part of As^o to evaporate. The Ga $2p_{3/2}$ spectra of the sample S1, S2, S3 are demonstrated in Fig. 4. For sample S1 and S2, the Ga 2p $_{3/2}$ peak are deconvoluted into two main peaks, which are deemed to correspond to Ga–As bond and Ga–O bonds. For sample S3, it's worth noting that except the Ga–As and Ga–O bond, a new peak located at 1117.78 eV has been detected, which may come from the Ga–S bond, indicating that GaAs surface has been passivated by $(NH_4)_2S$ solution. The S 2p spectrum in inset of Fig. 4 demonstrates that element S has been introduced into GaAs surface effectively after S-passivation treatment. With the advancement of S-passivation process, it can be noted easily that the binding energy of Ga–O shifts from 1118.21 eV to 1118.47 eV and to 1118.66 eV, which can be due to the change of chemical state of Ga–O bond [25]. Meanwhile, the decreases of the intensity of Ga–O bond,

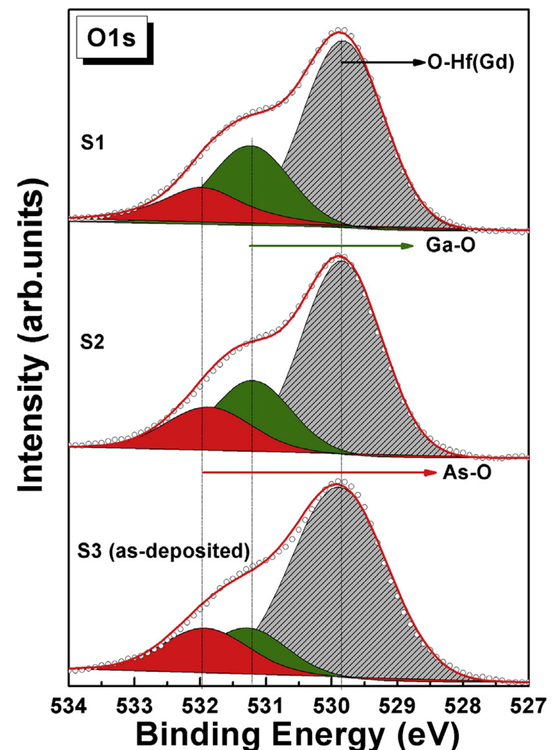

Fig. 5. O 1s core-level XPS spectra of S1, S2, S3.

indicating the S-passivation is a feasible treatment to optimize the GaAs surface. From O 1s core level spectra shown in Fig. 5, it can be seen that all spectra are deconvoluted into three peaks located at binding energies of 529.8 eV, 531.21 eV, and 531.97 eV, which may come from O–Hf(Gd), Ga–O, and As–O, respectively. From Fig. 5, the intensity of Ga–O bond constantly decreases with the boost of S-passivation process, which is in good agreement with the result of Ga $2p_{3/2}$. At the same time, the change of the intensity of As–O bond also correspond to the result of As 3d, almost remain unchanged. The profiles of Hf 4f spectra are given in Fig. 6. For all sample S1, S2, S3, Hf 4f could be decomposed into two contributions of Hf $4f_{5/2}$ and Hf$4f_{7/2}$, which can be fitted well by spin orbit doublet with an energy of 1.5 eV [26]. For the sample S1, S2, S3, the two peaks of Hf $4f_{5/2}$ and Hf$4f_{7/2}$ located at 16.23 eV and 17.87 eV with the spin-orbit splitting of 1.64eV. There is almost no energy shift with the evolution of S-passivation process, indicating there is no existence of metallic salt which is similar to the silicate component. Based on the profiles of As 3d, Ga $2p_{3/2}$, O1s and Hf 4f spectra, it is concluded that the arsenic oxide, gallium oxide and elemental arsenic are dominantly formed between the HGO thin film and GaAs substrate. The acid cleaning and S-passivation both contribute to optimize the surface of GaAs substrate.

3.2. Electrical measurement of S-passivation process

Fig. 7 shows the *C-V* characteristics of three samples measured at 1 MHz. There are no apparent difference in values of accumulation capacitance (C_{ox}) of S1, S2, S3, which may be due to the negligible change in the dielectric constant. The relative dielectric constant (k) of HGO thin films are obtained from the accumulation capacitance, which are 17.97, 19.98, 18.77 for the sample S1, S2, S3, respectively. The similar values of equivalent oxide thickness (EOT) are also found in Table 1. Additionally, it can be noted that there is a large negative shift of *C-V* curves for S1, S2, S3, which can be ascribed to the decrease in value of flat band voltage V_{fb}. The values of V_{fb}, the density of oxide charge O_{ox}, the hysteresis ΔV_{fb} and the border trapped oxide charge density N_{bt} can also extract from *C-V* curves, as shown in Table 1. The positive V_{fb} indicates that there much negative oxide charges while less positive oxide changes in the films and/or at the interface, which may be attributed to more negatively charged interstitial oxygen atoms in the film and/or at interface [27]. Compared to S1, the sample S3 shows an obvious negative V_{fb} shift, which indicates the decreasing of negative oxide

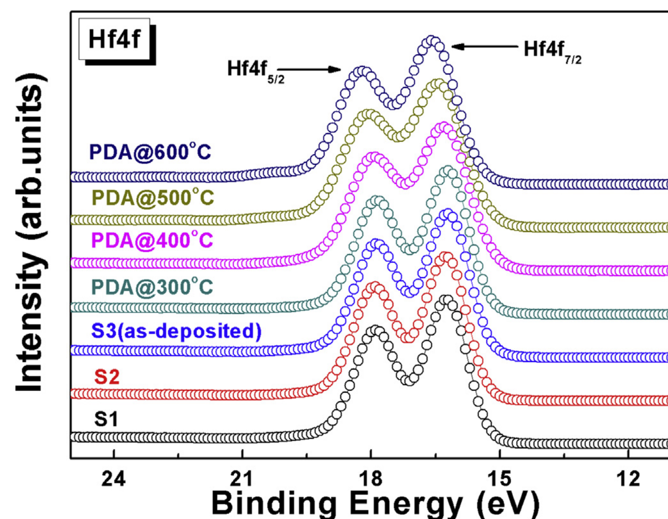

Fig. 6. Hf 4f core-level XPS spectra of S1, S2, S3 and various annealing temperature.

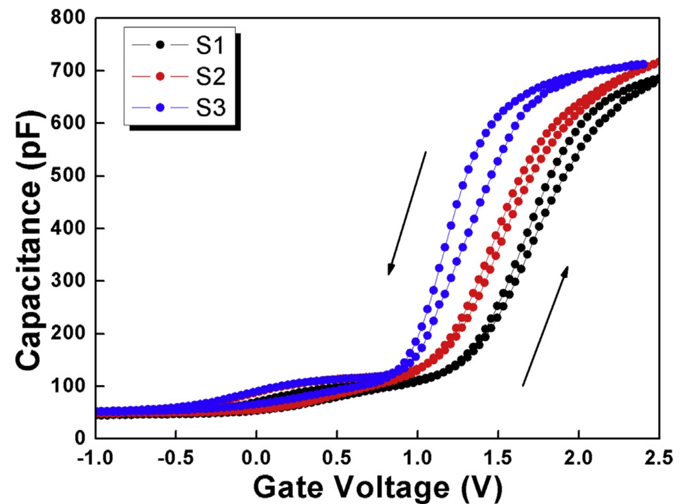

Fig. 7. Capacitance–voltage (*C–V*) characteristics curves of S1, S2, S3.

changes and the generation of more positive charges in the oxide layer and/or at the interface. The O_{ox} is calculated by follow relation: $O_{ox} = -C_{ox}(V_{fb} - \varphi_{ms})/Aq$, in which the φ_{ms} is the work function between Al electrode and GaAs substrate, A is Al electrode area. The negative O_{ox} may be related to acceptor-like interface and near-interface traps [28]. Compared with S1, S2, the sample S3 has the lowest O_{ox} with the value of -8.38×10^{12} cm^{-2}. Continuously reduction of negative O_{ox} suggest that the improvement of interface quality. The root cause of hysteresis ΔV_{fb} is difference in gate bias at which electrons fill the traps and escape from the traps, or the difference between the capture and emission times of the border traps [29]. The ΔV_{fb} value of the sample S2 are less than S1, however, the biggest ΔV_{fb} value is S3. The difference in hysteresis ΔV_{fb} is primarily ascribed to the difference in border trapped oxide charge (N_{bt}). The N_{bt} given by the expression: $N_{bt} = -C_{\max}\Delta V_{fb}/Aq$. The sample S3 has the high N_{bt} value of 1.54×10^{-4} cm^{-2} corresponding to the biggest ΔV_{fb} value. It may be due to the HGO/S-GaAs interface exist some dangling bond of S atom, which can result from the interface trap-assisted tunneling. In addition, apparent bump of *C-V* curves of all samples have been observed at inversion region, suggest that relatively higher interface state exist at the HGO/GaAs interface. The leakage current density as a function of the applied bias voltage for S1, S2, S3 are demonstrated in Fig. 8. It can be observed that the sample S3 through organic cleaning, acid cleaning and S-passivation possess the smallest leakage density of about 1.54×10^{-4} A/cm^2 at 1 V, which can be attributed to the best interface quality.

Based on the result of XPS and electrical measurement, S-passivation have a positive effect on the decreases of interface species (As–O, Ga–O, As^o) and the performance promotion of MOS devices.

3.3. XPS analysis of rapid thermal annealing

The XPS analyses for the HGO/S-GaAs interfaces were carried out to investigate the effect of the post-deposition rapid thermal annealing temperature on the interfacial component changes. For the deconvolution of spectra, the Shirley method is selected to subtract the inelastic background. According to the previous XPS results, the large amounts of elemental As^o and native oxides are covered on the as-deposited HGO thin film/GaAs interface, indicating that the surface species can not be removed only by pre-cleaning. However, it is reported that the surface species are the

Table 1
Parameters of the MOS capacitors extracted from ***C*–*V*** curves.

Samples	C_{ox} (pF)	Eot (nm)	K	C_{fb} (pF)	V_{fb} (V)	O_{ox} (cm^{-2})	ΔV_{fb} (V)	N_{bt} (cm^{-2})	J (A/cm^2)
S1	682	3.58	17.97	543.98	1.99	-1.06×10^{13}	−0.09	5.45×10^{11}	1.19×10^{-3}
S2	714	3.41	19.98	563.80	1.84	-1.02×10^{13}	−0.07	4.42×10^{11}	3.30×10^{-4}
S3 (As-deposited)	712	3.43	18.77	562.92	1.56	-8.38×10^{12}	−0.17	1.07×10^{12}	1.54×10^{-4}
PDA@500 °C	710	3.43	16.37	561.65	1.37	-7.16×10^{12}	−0.11	6.90×10^{11}	4.07×10^{-4}
PDA@600 °C	717	3.40	16.72	566.00	1.19	-6.09×10^{12}	0.04	-2.54×10^{11}	1.54×10^{-5}

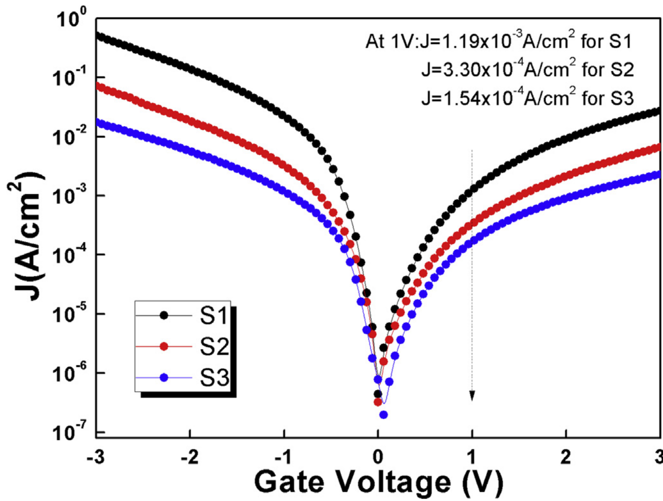

Fig. 8. Leakage current density–gate voltage (*J*–*V*) characteristics curves of S1, S2, S3.

main root of Fermi level pinning in GaAs MOS devices, especially the elemental As° and Ga oxides [30,31].

Figs. 9 and 10 describe the As 3d and Ga $2p_{3/2}$ core-level spectra. Based on Figs. 9 and 10, it can be noted that more Ga oxides and elemental As° exist at the HGO/GaAs interface with lowering annealing temperature. With the increase in annealing temperature, reduction in Ga oxides and elemental As° have been observed. When the annealing temperature increase to 600 °C, Ga oxides and elemental As° have been fully removed. However, the amount of As–O bond just presents a slight reduction with increasing the annealing temperature. Yang et al. reported the thermal treatment effect of Gd_2O_3/GaAs interface, the decomposition of As–O with the increasing temperature was observed [32]. Our experimental results are not accordance with the report, which may be due to the different high-k thin film and the different deposition process. Further detailed studies need to do to figure out the reason why the As–O bond only have the slight decrease at the higher annealing temperature. Additionally, judging from the As 3d spectra shown in Fig. 9, the Ga–As bonds shift toward a higher binding energy with the increase in annealing temperature. The same peak shift of Ga $2p_{3/2}$ and Hf 4f shown in Fig. 6 was also observed, indicating that a Fermi level shift toward a flat band condition occurs by annealing

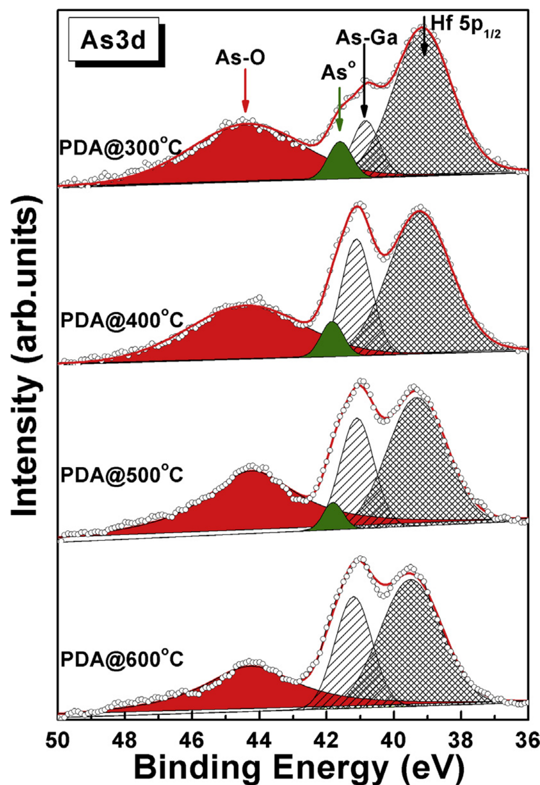

Fig. 9. As 3d XPS photoemission spectra of the HGO/GaAs gate stack annealed at various temperature.

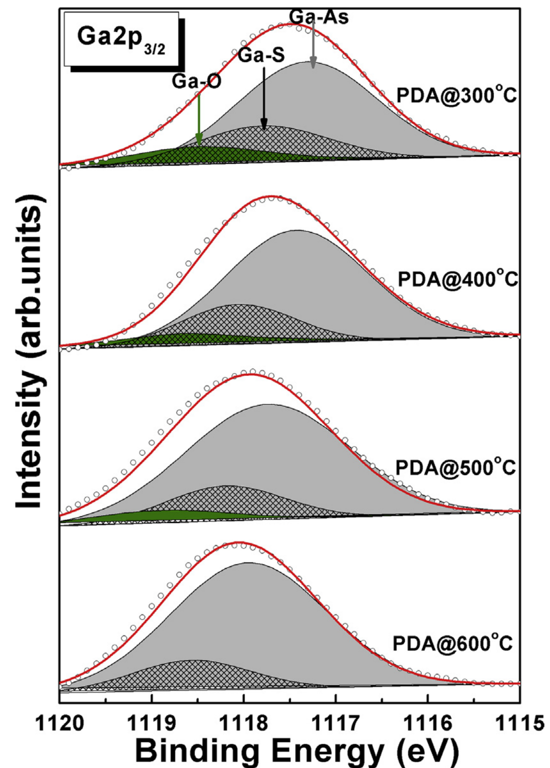

Fig. 10. Ga 2p $_{3/2}$ XPS photoemission spectra of the HGO/GaAs gate stack annealed at various temperature.

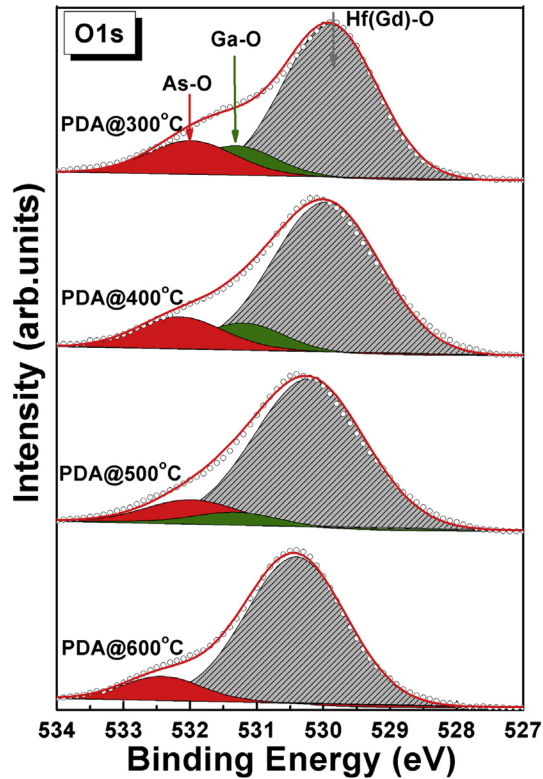

Fig. 11. O 1s XPS photoemission spectra of the HGO/GaAs gate stack annealed at various temperature.

[33]. From Fig. 10, the formation of Ga—S bond for all samples would contribute to the reduction of energy state in the band gap and the enhancement of resistance against the oxidation for further processes [32]. In order to verify the previous conclusions, O 1s spectra, given in Fig. 11, have been paid more investigation. Under lower annealing temperature, As and Ga oxides still exist. With increasing the annealing temperature, the amount of GaO_x decreases and disappears with the annealing temperature of 600 °C. However, although the reduction in amount for AsO_x, the complete removal of AsO_x has not been observed. Based on above XPS analyses, it can be concluded that the surface species can be modulated effectively by controlling the appropriate annealing temperature.

3.4. Electrical measurement of rapid thermal annealing

The interfacial changes are closely correlated with the electrical properties. Fig. 12 depicts the typical high-frequency (1 MHz) *C-V* characteristics of MOS capacitors based on HGO high-k gate dielectrics as a function of annealing temperature. Seen from Fig. 12, the *C-V* curves present a good MOS-type behavior with apparent accumulation, depletion, inversion regions. Especially, the 600°C-annealed *C-V* curves presents the sharpest transition from the depletion to the accumulation region, which owing to the smallest flat band voltage V_{fb} and the smallest hysteresis ΔV_{fb} with the value of 1.19 and 0.04, respectively, shown in Table 1. From Fig. 12, it can be noted that the "stretched out" effect is constantly decreased with the increase of annealing temperature, which directly attribute to the reduction in border trapped oxide charge (N_{bt}) given in Table 1. Compared to the as-deposited sample, the 500°C-annealed and the 600°C-annealed samples show a slight negative V_{fb} shift, which reflects the decrease of oxide charge density. Additionally, it is worth noting that the as-deposited *C-V* curve has an evident

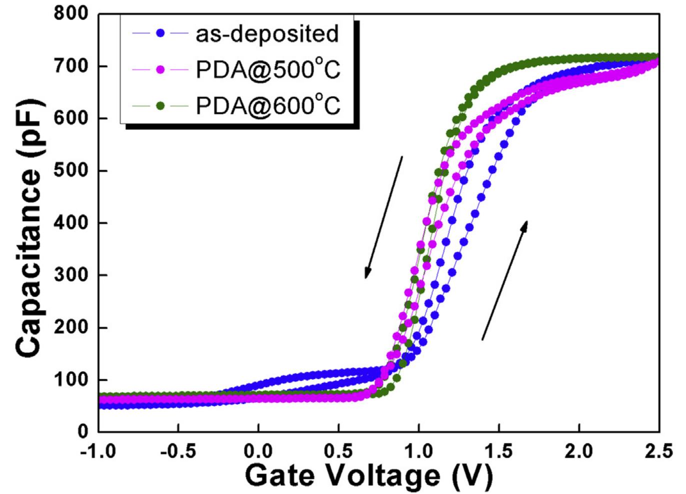

Fig. 12. High frequency (1 MHz) capacitance-voltage curves of HGO/GaAs gate stacks annealed at different temperature.

bump at inversion region and the 500°C-annealed *C-V* curve has an apparent bend at accumulation region, the abnormal shape indicating the existence of higher interface state at the HGO/GaAs interface. However, when the annealing temperature is increased to 600 °C, both the bump and bend disappear, indicate the improvement of interface quality. It may be due to the 600°C-annealed sample embrace the minimum interface species, confirmed by previous XPS results. In addition, according to the C_{ox}, the permittivity K can be extracted, which are 18.77, 16.37 and 16.71 corresponding to the equivalent oxide thickness (EOT) 3.43, 3.43 and 3.40 for as-deposited, the 500°C-annealed and the 600°C-annealed HGO thin film, respectively. The 600°C-annealed sample possess the smallest EOT and suitable dielectric constant. Fig. 13 shows the leakage current density versus voltage for HGO/GaAs MOS capacitors annealed at various temperatures under gate injection and substrate injection. The leakage current density for the as-deposited and annealed samples at 300 °C and 500 °C, are about 1.54×10^{-4} A/cm^2, 4.07×10^{-4} A/cm^2, 1.54×10^{-5} A/cm^2, respectively. It is the clear that 600°C-annealed HGO film has lower leakage current density than others, indicating the disappearance of numerous oxide charge and trap after appropriate temperature annealing.

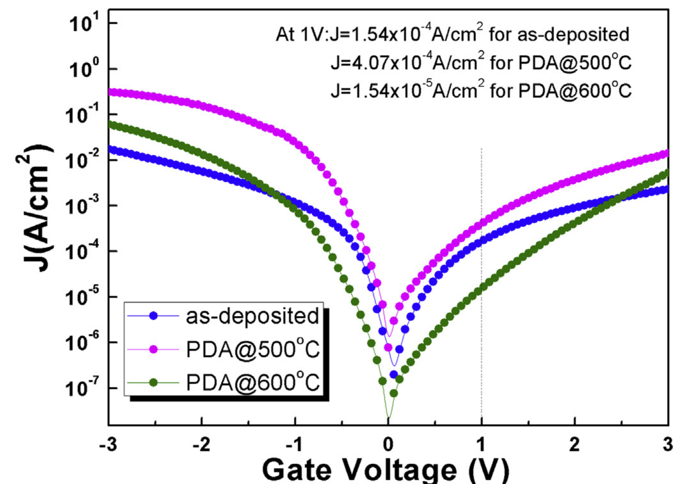

Fig. 13. *J-V* characteristics of MOS capacitors with HGO/GaAs gate stacks as a function of annealing temperature.

4. Conclusion

Surface passivation of GaAs wafer by using $(NH_4)_2S$ solution prior to HGO deposition and post-deposition thermal annealing have been carried out to reduce the surface species of GaAs wafers. XPS results of surface passivation demonstrate that the only acid cleaning is not enough to remove the native oxides. The native oxides and elemental As^o unavoidably formed between HGO thin films and GaAs substrate. Sulfur passivation decrease the native oxide GaO_x and elemental As^o but not effect to AsO_x. And those effect clearly improve the *C-V* characteristics and reduce the leakage current density. On the other hand, there is obvious composition changes after rapid thermal annealing based on XPS analyses. The 600°C-annealed HGO thin films fully remove the native oxides GaO_x and elemental As^o at the HGO/S-passivated GaAs interface, but no effect to AsO_x. The reason why the AsO_x almost remain unchanged even if at the higher temperature are need to further study. According to high frequency (1 MHZ) *C-V* and *J-V*, 600°C-annealed HGO thin films has the moderate dielectric constant 16.72, the smallest flat band voltage V_{fb} 1.19 V and hysteresis ΔV_{fb} 0.04 V corresponding to the smallest oxide charge density O_{ox} 6.09×10^{12} cm^{-2} and border trapped oxide charge density N_b 2.54×10^{11} cm^{-2} and the lowest leakage current density 1.54×10^{-5} A/cm^2. In conclusion, both the sulfur passivation and heat treatment can effectively suppress the regrowth of interface species.

Acknowledgments

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