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A high-speed data acquisition system based on FPGA for tokamak

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The Experimental Advanced Superconducting Tokamak (EAST) device aims to achieve a steady-state and long-pulse discharge over 1000 s. An embedded high-speed data acquisition system based on a field-programmable gate array (FPGA) for EAST is designed in this study. A cyclone FPGA is used as the master chip, and a TI's analog-to-digital conversion (ADC) chip is used to complete ADC. One acquisition system board consists of four ADC chips. The acquired data are compressed and stored into a disk array through a Peripheral Component Interconnect (PCI) Express interface and then uploaded to the data server. One board can collect the signals of eight channels synchronously. A number of such boards can be used to collect additional channel signals. Experimental results show that the system can reach 80 MSps and the sampling precision can reach 12 bits with 1250 s continuous sampling. The system integrates signal conditioning, data acquisition, and data processing into a single board and provides an architecture with high integration and portability levels. *Published by AIP Publishing.*
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I. INTRODUCTION

The tokamak device is an important and prospective device meant for achieving long-time steady-state controlled nuclear fusion. The Experimental Advanced Superconducting Tokamak (EAST) is a full-superconducting tokomak device designed and developed by the Institute of Plasma Physics, Chinese Academy of Sciences, and it aims to achieve a long-pulse discharge of up to 1000 s with 1.0 MA plasma current.[1,2] Typically, more than 1000 channels' data, such as experimental engineering data, electromagnetic measurement data, and diagnostic data, need to be collected during an EAST experiment. For certain diagnostic data, the data acquisition system's sampling rate ranges from 10 kSps to 10 MSps or even higher, depending on the requirements of the physical diagnosis system.[3,4]

Conventional data acquisition systems in EAST, such as computer-automated measurement and control (CAMAC) digitizers and new Peripheral Component Interconnect (PCI) cards, are usually adopted for short-pulse discharge, but their sampling rates and total acquisition durations are typically limited due to the restricted capacity of the storage media on the board.[5] The sampling rate of these conventional systems may be slowed to allow their use for long-time plasma discharge, thereby decreasing accuracy and omitting certain detailed physical information of the signals.[6] Therefore, for long-pulse experiments of EAST with a duration up to 1000 s, real-time data acquisition will be indispensable. The hardware of data acquisition systems of EAST currently includes signal conditioning, interconnecting, and data acquisition devices that are based on PCI, PCI extensions for Instrumentation (PXI), Industry Standard Architecture (ISA), Extended Industry Standard Architecture (EISA), and Virtual Instrument Software Architecture (VISA).[7–9] They are independent devices and interconnected with various cables. As a result of the long cables and the unreliable connectivity between independent systems, signals have attenuation before signals are acquired, and noises are imported.

This work presents an embedded data acquisition system with high-speed and long-time acquisition and is based on field-programmable gate array (FPGA) technology, which can collect, convert, and store multichannel signals in real time. This work aims to obtain a high-integration-level architecture that allows signals to be simultaneously acquired according to the external triggers with a high sampling rate of up to 80 MSps, processed, and stored to be used in long-time fusion devices. The main characteristics of the system are described in the following Secs. II through V.

II. HARDWARE STRUCTURE

A. Overview of the system

The proposed data acquisition system integrates data acquisition, compressing, and processing functions into a signal board on the basis of the embedded system. Each FPGA-based data acquisition system consists of four analog-to-digital conversion (ADC) chips; that is, it has eight simultaneously acquiring channels. Such ADC chips work alternately through controlling the clock module. The collected data are compressed and written to the disk array through the PCI Express (PCIE) interface, and these data can then be accessed and

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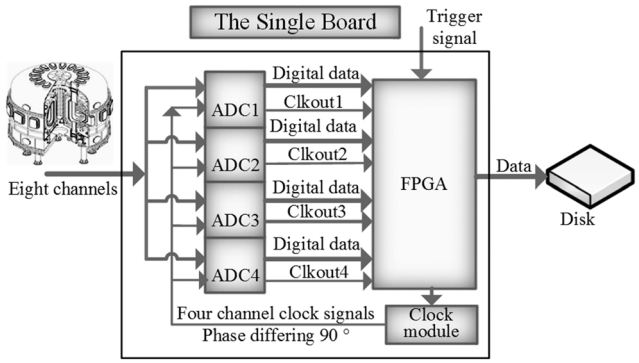

FIG. 1. Hardware structure of the embedded data acquisition system.

transmitted to the data server. The system integrates into the single board and provides an architecture with high integration and portability levels. Each FPGA-based acquisition system can collect eight different signals; thus, the use of multiple systems can yield more channels' data acquisition capabilities than conventional systems. Figure 1 shows the hardware architecture of the proposed system. Its hardware consists of four ADC chips (ADC1, ADC2, ADC3, and ADC4), a clock module, an FPGA, a storage module, and a power module.

The FPGA, as the master chip used to control ADC chips and realize data transmission and data storage, is the core chip of the system. In this study, the FPGA is a series of cyclone IV GX of EP4CGX30F484, whose transmitter (Tx) speed is up to 840 Mbps and receiver (Rx) speed is up to 875 Mbps, with a low-voltage differential signaling (LVDS) interface. A dedicated hard core intellectual property (IP) for PCIE supports ×1, ×2, and ×4 channels, thus allowing the convenient transfer of data to the disk array. When receiving the trigger signal, the system starts to collect, convert, and store the data.

The TI's ADS 5271, which has a 12-bit resolution ratio and eight channels with a sample rate of up to 50 MSps, is used in this design. Four ADCs comprise a data acquisition node, and each ADC has the same sampling rate and the same clock signal frequency, which is the highest frequency (up to 20 MHz), with a phase difference of 90° in order. The National Semiconductor's clock generation core LMK61A2-312M is used as the clock chip, which has the maximum output clock signal that can reach 312.5 MHz. The clock chip LMK61A2-312M outputs only one LVDS, but a four-channel phase difference of 90° clock signals is used as the ADC clock signal. The clock distribution chip LMK01010 is used to configure the clock signal to obtain the four clock signals required to achieve the design request. According to this design, the maximum sampling rate can be multiplied four times through multiplex and be up to 80 MHz. The ADC can collect eight different signals by its eight channels synchronously. The clock module is used to generate the clock signals required by the system for the ADCs and the FPGA. The disk is used to store the collected data.

An Intel DC P3608 with PCIE interface, which has 1.6 TB of storage capacity, write speed of up to 3000 MB/s, and read speed of up to 5000 MB/s, is used to meet the demand of data storage. Its continuous sampling time can reach 1250 s when eight signal types are simultaneously sampled and stored at the highest speed.

B. Clock module design

1. Clock distribution chip

The use of an external clock chip provides a stable clock signal to the system. Hence, this study selects the National Semiconductor's clock chip LMK61A2-312M to generate clock signals for each ADC of up to 20 MSps. The clock chip LMK61A2-312M outputs only one LVDS, but the ADC's sampling method is the four-piece alternating sampling; therefore, a four-channel phase difference of 90° clock signals is required. The clock distribution chip LMK01010 is used to configure the clock signal to generate the four clock signals required to meet the design demand.

2. Clock configuration circuit

Figure 2 shows the module of the clock configuration circuit. Ports 1–5 of the FPGA are used to complete the configuration of the clock chip, and Fout outputs the required frequency of the clock signal. Certain ports in LMK61A2-312M are described as follows. DATA is the input port of serial data (SDATA), and the most-significant bit (MSB) comprises the first and the last four bits constituting the control and register selection bits. CLK is the input port of the clock signal with the data entering the shift register at the rising edge of the clock. LE is the enable input port. When LE becomes high voltage, the data are loaded from the shift register to the latch register. CE is the chip select (CS) input port. When CE is high, LMX2531 turns on the bits of internal power controlling. Fout is a voltage-controlled oscillator-buffered radio frequency output, and Ftest/LD is the multilevel output port of Complementary Metal Oxide Semiconductor (CMOS).

In the LMK01010 chip, LEuWire is the port of the latch signal. CLKuWire is the clock input port, and DATAuWire is the input port of configuration data and used to configure the chip working mode to generate the required clock

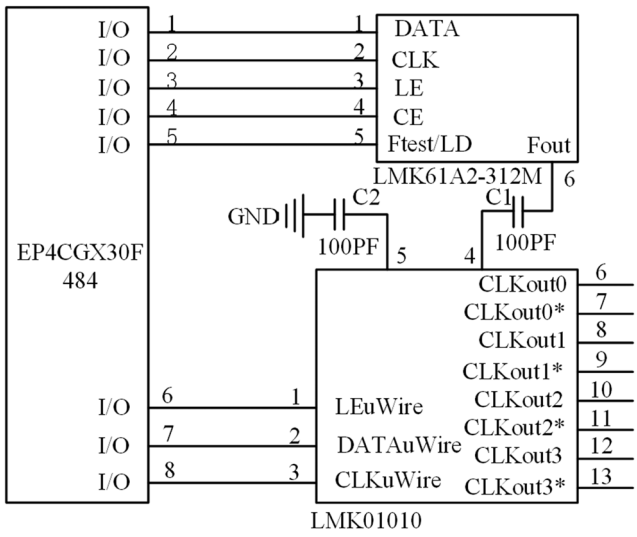

FIG. 2. Clock configuration module.

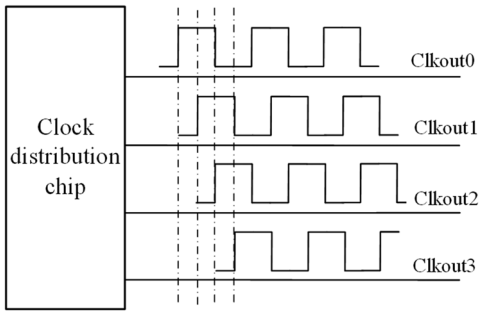

FIG. 3. Four-channel clock signals.

signal and connected to ports 6–8 of the FPGA. When LEuWire becomes low voltage, the data are latched at the falling edge of CLKuWire and then moved into the internal registers of LMK01010 at the rising edge of CLKuWire. CLKout0, CLKout0*; CLKout1, CLKout1*; CLKout2, CLKout2*; and CLKout3, CLKout3* are the four pairs of clock signals. As shown in Fig. 3, the clock distribution chip outputs four-channel clock signals, Clkout0, Clkout1, Clkout2, and Clkout3, with phases that differ from one another with 90° in order. Such signals are connected to four ADCs to achieve alternating sampling.

C. ADC module design

ADC chips are used to convert analog signals into digital data. ADC chips typically have monolithic single-channel and multichannel characters. This design aims to achieve the highest sampling rate of 80 MSps. Thus, several methods are adopted for the use of ADC chips. The first method is to utilize a single-channel ADC, which requires a single ADC channel with a sampling rate of 80 MSps. The second method is the use of a multichip, multichannel ADC, which acquires the final sampling rate by alternate sampling. The third method is to use a multichip, single-channel ADC, which also generates the final sampling rate by alternate sampling too. This study uses the second method to acquire the required sampling rate; four low-rate ADC chips are adopted, and we select TI's ADS5271 as ADC chips.

Four ADC chips are connected to the FPGA chip EP4CGX30F484. Figure 4 shows the part of the circuit design of ADC sampling. In the module, IN [0: 7] p and IN [0: 7] n are the LVDS channels for eight analog signals. CLK [0: 3] and CLK [0: 3] * are the four pairs of clock signals with phases that differ from one another by 90° in order and are connected to the four output ports CLKout [0: 3] from the clock distribution chip LMK01010. OUT [0: 7] p and OUT [0: 7] n are the output ports with digital signals converted by the ADC chips. CS, serial data clock (SCLK), and SDATA are used to configure the ADC chips and read digital data. According to the timing logic diagram of an ADC chip seen from ADC data sheets, CS is the port of chip selection. The chip works with the low voltage of the CS port. SCLK is the input port of the serial data clock. SDATA is the input port of serial data. The next serial data are ready to send at the falling edge of SCLK, and then the serial data are sent at the rising edge of SCLK.

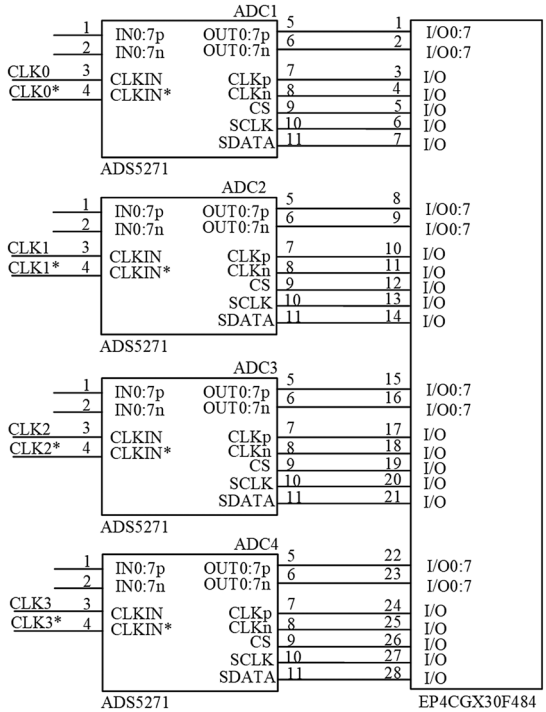

FIG. 4. Structure of the ADC module.

III. SOFTWARE DESIGN

A. Software structure

The program is written in Verilog HDL. Figure 5 shows the program workflow of the system. The system initializes the FPGA and generates different signals to configure the clock module and ADC chips. After receiving the trigger, the system collects data, and the data are compressed and transmitted to the disk. The data server can access and process the obtained data at any time.

B. Data compression

Various diagnostic signals need to be collected during the EAST experiment. The sampling rate usually ranges from kSps to MSps, and hence, a large amount of data needs to be collected. Lempel-Ziv-Oberhumer (LZO), a real-time data compressor, is adopted to decrease the data amount. The LZO algorithm is a fast lossless data compression and decompression algorithms.[10,11] The LZO library was originally written in ANSI C, and LZO currently has Perl, Python, and Java versions. The processing speed is the design principle of LZO. The LZO decompression speed is generally faster than its compression speed, but the compression ratio can be freely adjusted as needed and does not affect the decompression speed. The decompression algorithm is simple and has no memory support, and LZO can provide lossless compression.

The design uses the Verilog language to implement the LZO algorithm and achieve data compression in the FPGA. The data compression module in the FPGA does not affect the data acquisition efficiency in the data compression due to the FPGA parallel processing mechanism. After the data acquisition of each time slice is completed, the data need to be transmitted and saved to the disk.

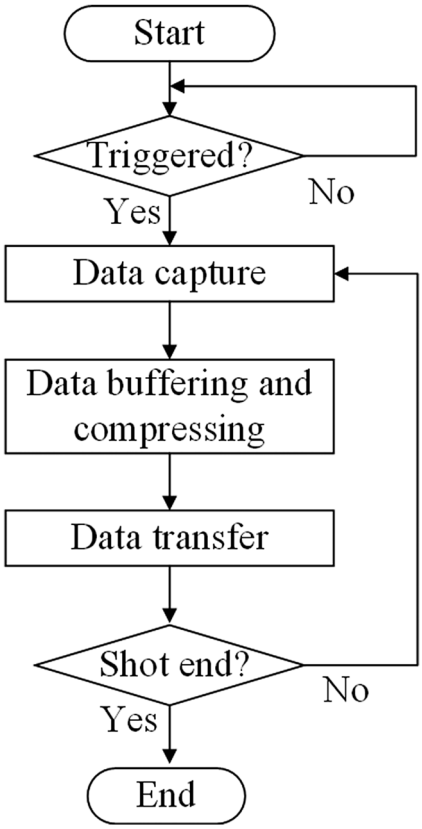

FIG. 5. Software workflow.

C. Data transmission

The compressed data are transferred to the disk via the PCIE ×4 interface. The FPGA used in this system provides the hard IP module for PCIE ×1, ×2, and ×4. High-speed end-to-end data transmission can therefore be achieved without the need to add to other dedicated PCIE protocol chips.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. ADC sampling simulation

The ADC chips start sampling after receiving the sampling command from the central control system. The FPGA core chip stores the data into the first in-first out (FIFO) buffer and then transfers these data to the disk. Figure 6 illustrates the result of a single-channel sampling simulation diagram. CLKout0 is the sampling clock. rst_n is the reset signal; the reset signal is actively high. The ADC collects data at the rising edge of CLKout0, and the collected data are moved into the internal buffer. The signal of ad_data_out is the same as that of ad_data_in, and this similarity indicates the data collection accuracy of the system.

B. Data multiplex simulation

Four-channel data with the same rate are acquired by the ADCs. The design uses an FPGA to multiplex these data into single-channel data and generate four times the sampling rate. Figure 7 shows the simulation result, in which four-piece ADC chips with 20 MSps sampling rate obtain a multiplex simulation signal. Thus, a sample rate of 80 MSps is obtained. CLKout0, CLKout1, CLKout2, and CLKout3 are the four-channel clock signals, and rst_n is the reset signal. ad_data_ina, ad_data_inb, ad_data_inc, and ad_data_ind are the data of the same channel of signal collected by four pieces of ADC chips. ad_data_out is the data-out port. When the CLKout0 is in the rising edge, the data in ad_data_ina are exported from the ad_data_out. By the same way, the CLKout1 is in the rising edge, and the data in ad_data_inb are exported from the ad_data_out, followed by a cycle. The essence of the multiplex is to collect data in the same sampling rate but at different times. As shown in Fig. 7, the collected data are not lost with the highest sampling rate, and the data are delayed by approximately 2 ns, which meets the design requirements. The experimental result shows that the system can reach 80 MSps and the sampling precision can reach 12 bits with the 1250 s continuous sampling.

C. Multichannel data acquisition

The data of over 1000 channels need to be collected during the EAST experiment. The system proposed in this paper integrates into a single board and provides an architecture with high integration and portability levels. One board can collect the signals of eight channels synchronously. Numerous FPGA boards can be used together for acquiring more channels' data to meet the multichannel demand. Figure 8 shows the system structure for multichannel data acquisition. FPGA-based data acquisition systems, controlled by the central control system, collect the signals of the EAST device in real time. The data

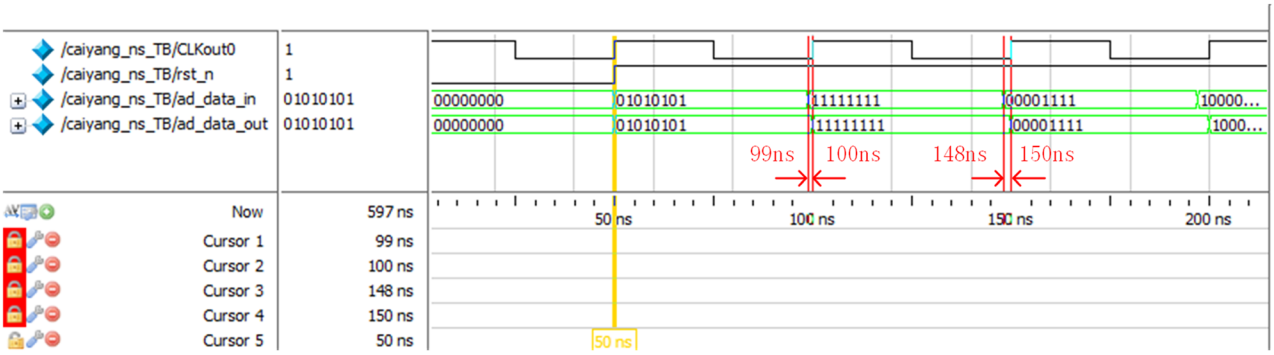

FIG. 6. The result of ADC sampling simulation.

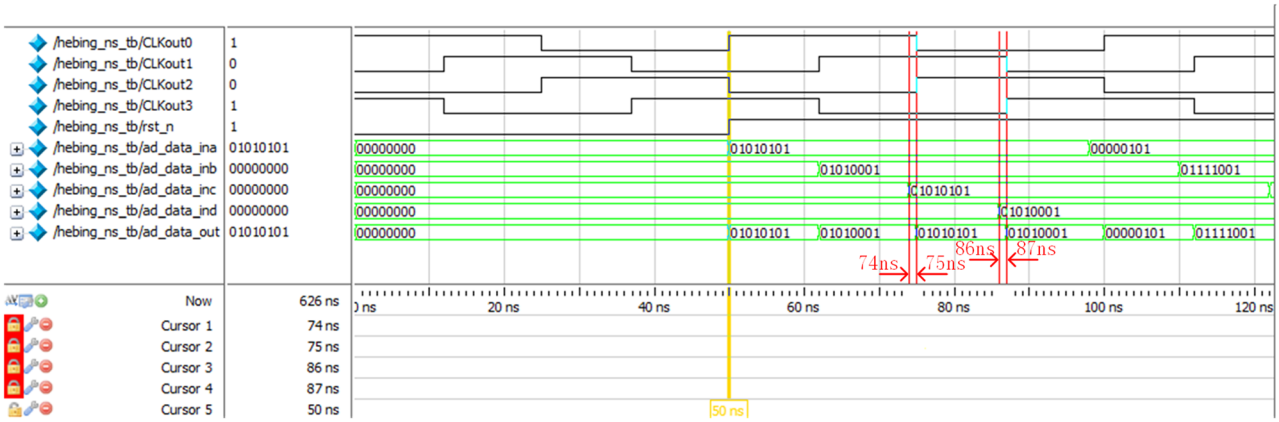

FIG. 7. The result of multiplex simulation.

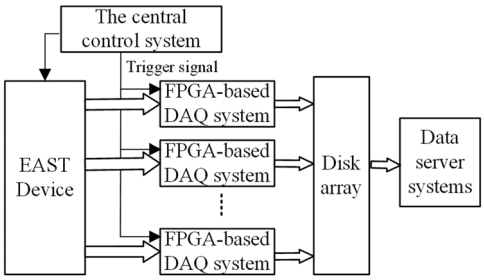

FIG. 8. Structure of multichannel data acquisition.

are converted and stored in the disk array, where they can be read by data servers. Such data can be easily accessed and used by operators and experimenters.

V. SUMMARY

A new high-speed FPGA-based data acquisition system for continuous data acquisition for long-time and steady-state operation of EAST was developed. The system's structure differs from that of a conventional data acquisition system; it integrates signal conversion, and data processing and transmission in one board. The system can continuously capture data at the highest sampling rate up to 80 MSps during more than 1250 s. New technologies, such as high-speed alternative ADC chips' data conversion, FPGA, and LZO technologies, are introduced into this system. To a certain degree, this system reduces the disturbance caused by the long-distance transmission of signals and the transmission among the system parts. An architecture with high integration and portability levels is provided. This system is highly flexible and reduces design cost. One board can collect the signals of eight channels synchronously. The highest sampling rate of the system can reach 80 MSps. The FPGA can be conveniently reprogrammed through Verilog HDL for changing the sampling rate according to acquisition demand. The proposed method provides a feasible solution for data collection in EAST experiments and other such applications.

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[1]Y. Liu, J. R. Luo, G. M. Li, Y. F. Zhu, and S. Li, Fusion Eng. Des. **82**, 339 (2007).
[2]S. Li, Y. Wu, G. Li, F. Wang, and Y. Zhu, IEEE Trans. Nucl. Sci. **57**, 696 (2010).
[3]Z. J. Chen, X. Y. Peng, X. Zhang, T. F. Du, Z. M. Hu, Z. Q. Cui, L. J. Ge, X. F. Xie, X. Yuan, G. Gorini, M. Nocente, M. Tardocchi, L. Q. Hu, G. Q. Zhong, S. Y. Lin, B. N. Wan, X. Q. Li, G. H. Zhang, J. X. Chen, and T. S. Fan, Rev. Sci. Instrum. **85**, 11D830 (2014).
[4]D. M. Liu, B. N. Wan, W. Z. Zhao, B. Shen, Y. G. He, B. Chen, J. Huang, and H. Q. Liu, Rev. Sci. Instrum. **85**, 11E826 (2014).
[5]J. C. Xu, L. Wang, G. S. Xu, G. N. Luo, D. M. Yao, Q. Li, L. Cao, L. Chen, W. Zhang, S. C. Liu, H. Q. Wang, M. N. Jia, W. Feng, G. Z. Deng, L. Q. Hu, B. N. Wan, J. Li, Y. W. Sun, and H. Y. Guo, Rev. Sci. Instrum. **87**, 083504 (2016).
[6]D. M. Liu, B. N. Wan, J. Li, Y. Wang, B. Shen, X. Z. Gong, and Y. G. He, Rev. Sci. Instrum. **87**, 11D839 (2016).
[7]F. Wang, G. M. Li, S. Li, Y. F. Zhu, and Y. Wang, IEEE Trans. Nucl. Sci. **57**, 669 (2010).
[8]W. Y. Xu, H. D. Xu, F. K. Liu, F. Hou, and Z. G. Wu, Fusion Eng. Des. **113**, 119 (2016).
[9]J. J. Patel, B. K. Shukla, N. Rajanbabu, H. Patel, P. Dhorajiya, D. Purohit, and K. Mankadiya, Fusion Eng. Des. **112**, 919 (2016).
[10]Z. Lin, J. R. Luo, G. M. Li, and D. L. Yue, Plasma Sci. Technol. **5**, 1939 (2003).
[11]Y. Liu, G. M. Li, Y. F. Zhu, and S. Li, Fusion Eng. Des. **86**, 151 (2011).