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Interface Modulation and Optimization of Electrical Properties of HfGdO/GaAs Gate Stacks by ALD-Derived Al_2O_3 Passivation Layer and Forming Gas Annealing

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Metal-oxide-semiconductor (MOS) capacitors with sputtering-deposited Gd-doped HfO_2(HGO) high k gate dielectric thin films and ALD-derived Al_2O_3 interfacial passivation layer were fabricated on GaAs substrates. The effects of the passivation layer and the forming gas annealing (FGA) temperature were explored by studying the interfacial chemical bonding states and electrical properties of HGO/GaAs and HGO/Al_2O_3/GaAs gate stacks via x-ray photoelectron spectroscopy (XPS), capacitance-voltage (*C*–*V*), and leakage current density-voltage (*J*–*V*) measurements. Results indicated that the MOS capacitors performances were enhanced by performing FGA. The electrical analysis revealed that the 300 °C-annealed Al/HGO/GaAs/Al MOS capacitor with 20 cycles Al_2O_3 passivation layer experienced improved electrical properties, with a dielectric constant of 44, a flat band voltage of 0.64 V, a hysteresis of 0.02 V corresponding to the oxide charge density of -6.2×10^{12} cm^2, border trapped oxide charge density of -3.02×10^{11} cm^2, a leakage current density 5.87×10^{-6} A/cm^2 at a bias voltage of 2 V. The low temperature (77–300 K) dependent detailed current conduction mechanisms (CCMs) of the 300 °C-annealed MOS capacitor at low temperatures were also systematically investigated. The optimized interface chemistry and the excellent electrical properties suggested that HGO/Al_2O_3/GaAs potential gate stacks could be applied in future III-V-based MOSFET devices.

1. Introduction

SiO_2 is one of the most popular semiconductors used in the modern electronics. It boasts high quality interface properties with a low interface state density (D_{it}) of less than 10^{10} cm^2 between SiO_2/Si.[1] In addition, SiO_2 boasts superior physical properties, including a relatively high band gap (≈8.9 eV), a suitable band offset (3.0–4.0 eV), a high breakdown electric field strength (≈15 MV cm^{-1}), and good thermal stability.[2] By 2019, integrated circuit products with a 16 nm characteristic size will be put in mass production, according to the International Technology Roadmap for Semiconductors. By then, the corresponding SiO_2 gate dielectric layer thickness is projected to be as small as 1 nm.[3] This will result in the gate leakage current increasing exponentially, due to the effect of the quantum tunneling effect. This occurs when the SiO_2 thickness decreases to the size of the atom, which facilitates the diffusion of impure ions and causes the device failure to function normally.[4] Dielectric materials with high dielectric constants (high-k) could be used as alternative gate dielectrics for SiO_2, since high-k gate dielectric material can obtain thicker physical thickness while maintaining the gate capacitance. This would effectively reduce the leakage current.[5] The Coulomb scatterings and the phonon scatterings of the interface between the high-k gate dielectric material and the channel material would result in a significant decrease in the channel mobility, which would detrimentally affect the speed of the complementary metal-oxide-semiconductor (CMOS) logic device.[6] Selecting suitable channel materials with high mobility is an effective solution. Among the III-V compound semiconductors, GaAs is considered an alternative channel material of Si for extending the performance limits of complementary metal-oxide-semiconductor field effect transistors (CMOSFETs) logic devices due to its higher band gap, higher carrier mobility, and smaller effective mass compared to those of Si or strained Si.[7,8] The surface and the interface of the binary GaAs semiconductor has a higher activity than Si, which can easily be oxidized and results in the higher D_{it}

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when exposed to air or other oxidation atmospheres. The high D_{it}, which is attributed to the interfacial layer of high-k/GaAs, results in Fermi level pinning and large frequency dispersion of the capacitance. This prevents the formation of the inversion or the accumulation layer of the CMOS devices.[9] The binding energy of the metal—oxygen bond in high-k gate dielectrics is much lower than that of Si—O bond in SiO_2. The oxygen atoms in the high-k gate dielectrics are easily diffused into the substrate, which leads to the increase of oxygen vacancies in the high-k gate dielectrics and the formation of an additional interface layer at the high-k/GaAs interface. For the successful realization of GaAs-based MOSFETs, control of the interfacial oxides on GaAs upon gate stack formation has been recently explored by using appropriate passivation treatment methods. There have been passivation treatments employed to reduce or remove interfacial oxides, such as chemical solution processing, introducing an interface control layer, and nitridation pretreatment. The chemical solution method primarily uses HF, $NH_3.H_2O$, $(NH_4)_2S$, and other solutions to clean the GaAs substrate. This allows the dangling bond on the substrate surface to be passivated by H, N, and S, which suppresses the adsorption of oxygen atoms on the surface of the substrate.[10,11] Introducing the passivation layer could result in the formation of the high-k/passivation layer/GaAs gate stack and prevent the mutual oxygen diffusion from the high-k gate dielectrics to GaAs substrate.[12–15] Nitridation pretreatment has been performed by annealing the GaAs substrate in an ammonia or nitrogen atmosphere in order to form the passivation layer, which halts the further oxidation of the substrate.[16,17]

Due to its large band gap, suitable band alignment, and good thermodynamic stability with Si, HfO_2 gate dielectrics have been regarded as potential candidates for high-k gate dielectrics to replace SiO_2 from 45 to 22 nm technology nodes by the Intel Corporation. Their moderate dielectric constants make Hf-based gate dielectrics limited for future CMOS devices scaling that have with an equivalent oxide thickness (EOT) below 1.0 nm. Fortunately, modification of Hf-based oxide dielectric via rare earth (RE) oxides, such as Gd_2O_3, are proven to increase permittivity, enlarge the band gap, balance the band offsets, reduce the defect states, and suppress oxygen vacancies of Hf-based oxide dielectrics. Although, there has been improvement in the interfacial chemistry and electrical properties, some serious drawbacks have been detected in the HfGdO/GaAs gate stack, including the formation of interface layer with higher defect states. This would lead to a higher oxygen vacancy density than that of SiO_2, which led to a higher leakage current, a lower carrier mobility, and a shift of threshold voltage. Therefore, the interface control and the exploration of the electrical properties of the HfGdO/GaAs stack requires further clarified.

The current study used Gd-doped HfO_2 (HGO) thin films as a high-k gate dielectric to decrease the oxygen vacancies in HfO_2 and reduce the gate leakage current. Sulfur passivation has been proven to be an effective passivation method,[18–20] so the combination of sulfur passivation and other passivation processes were chosen. The electrical performance of the GaAs-based MOS capacitors was improved with a three step method. The diluted HBr and $(NH_4)_2S$ solution was used to reduce the native oxides of the GaAs surface and promote the passivation of the surface dangling bonds of GaAs, which prevented oxidation. Then, the atomic layer deposition (ALD) Al_2O_3 passivation layer was introduced to the surface of the passivated GaAs substrate to suppress the mutual diffusion. The interfacial layer was formed, since Al_2O_3 possessed a lower ion permeability, a higher thermal stability, a band gap of 8.8 eV, and a suitable band offset (2.8–4.9 eV) relative to GaAs. The optimized electrical properties were obtained by forming gas annealing (FGA, 5% H_2 + 95% N_2) for the GaAs MOS capacitors based on $HGO/Al_2O_3/GaAs$ gate stacks. More attention have been paid to investigate the evolution of the interfacial chemical states and electrical properties in the $Al/HGO/Al_2O_3/GaAs$ MOS structure as functions of ALD-derived Al_2O_3 growth cycles and forming gas annealing temperature by X-ray photoelectron spectroscopy (XPS), UV–vis spectroscopy, high frequency capacitance–voltage (*C*–*V*), current density voltage (*J*–*V*) measurements, and low-temperature leakage current conduction mechanism.

2. Results and Discussion

2.1. Interface Bonding State Characteristics

XPS analysis was performed to explore the interfacial chemical composition and the respective chemical states of HGO/GaAs gate stacks with different ALD cycles Al_2O_3 passivation layer. The S1, S2, and S3 represented 0, 10, and 20 cycles of the passivation layer, respectively. Figure S1a (Supporting Information) displays the survey spectrum of the three samples at a binding energy ranging from 0 to 1300 eV. Hf, Gd, O, Ga, As, and C were detected, suggesting that the films escaped from other contaminations and also confirmed that Gd was successfully incorporated into the HfO_2 gate dielectrics. Due to the relative lower intensity, Al and S were difficult to observe. The high-resolution Al 2p and S 2p core-level spectra are presented in Figure S1b,c in the Supporting Information, respectively. This finding suggested the presence of Al and S. Table S1 (Supporting Information) illustrates the specific atomic ratio between Hf:Gd in the films, which is as similar to that of sputtering target. The atomic percentage of Ga was consistently higher than As in samples S1, S2, and S3 (Table S1, Supporting Information). This could cause the appearance of arsenic vacancy and become inclined to act as the acceptor in the forbidden band.[21]

The As 3d high resolution XPS spectra of three samples is shown in **Figure 1**a. All samples were deconvoluted into six peaks, which corresponded to Hf $5p_{1/2}$ (≈38.88 eV), As-Ga (≈40.52 eV), elemental arsenic As^{o} (≈41.3 eV), As^{1+}oxide (≈43.12 eV), As^{3+}oxide (≈44.65), and As^{5+}oxide (≈46.16), respectively. Note, the introduction of Al_2O_3 passivation layer seemed to improve the HGO/GaAs interface, which was confirmed by the reduction of the arsenic oxides (As^{1+} and As^{3+} oxides) and As^{o}. The peak area percentages of arsenic oxides are listed in **Table 1**. Sample S3 with 20 cycles Al_2O_3 passivation layer effectively blocked the interfacial reactions between the interdiffused oxygen impurities and the out-diffused atomic As. This suppressed the formation of As oxide.[22] Trimethylaluminium $[Al(CH_3)_3]$ (TMA) precursor had a good self-cleaning effect on GaAs surface during the deposition process of Al_2O_3 thin films. According to Ligand exchange system,[23] the following reaction could occur during the ALD deposition process: $2Al(CH_3)_3 + As_2O_3 \rightarrow Al_2O_3 + 2AS(CH_3)_3$,

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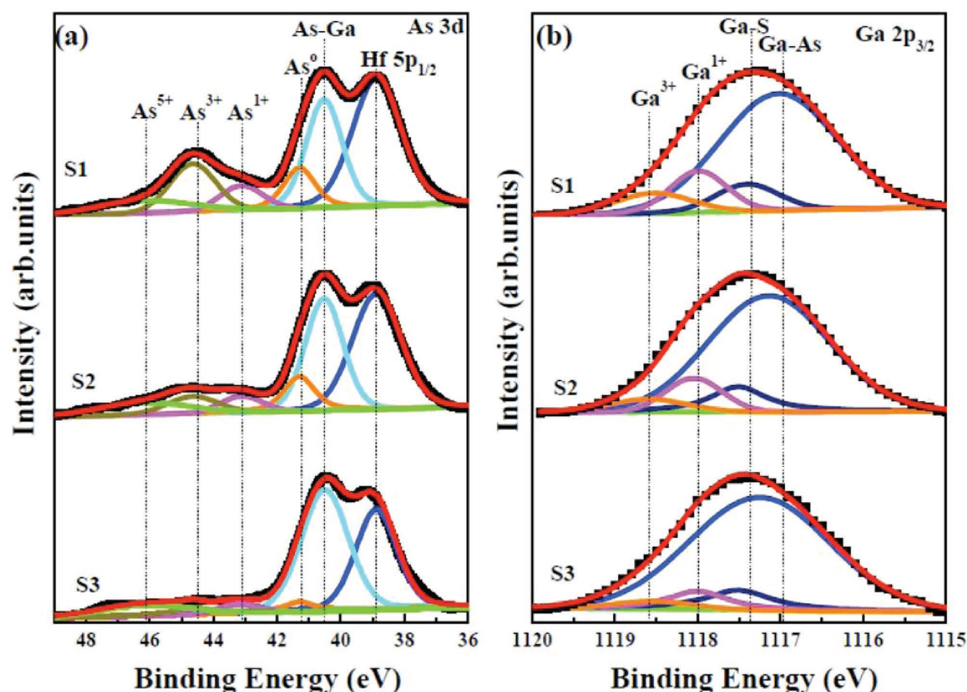

Figure 1. The a) As 3d and b) Ga 2p core-level XPS spectra of S1, S2, and S3.

which would be beneficial to the reduction of As^{3+} oxides and would produce the volatile substance. The double effect of the Al_2O_3 passivation layer and the above reaction made the As^{3+} oxides possess the maximum reduction, as shown in Figure 1a and **Table 2**. Suri et al. reported that As° is unstable on heated GaAs surfaces and has a tendency to evaporate.[24] Reduction in As° could be a result of the 200 °C ALD deposition temperature, which caused causing parts of the As° to evaporate. The reason why the As^{5+}oxides almost remained nearly unchanged, even if the introduction of Al_2O_3 passivation, remains unknown and more study is needed.

The Ga $2p_{3/2}$ high resolution spectra of the three samples are depicted in Figure 1b. All spectra were deconvoluted into four peaks located at binding energies of 1116.99, 1117.46, 1117.99, and 1118.54 eV, which corresponded to the Ga-As, Ga-S, Ga^{1+}oxides, and Ga^{3+}oxides, respectively. The relative peak area percentages of the three samples are presented in **Table 3**. The intensity and the relative area percentage of the Ga—S bond remained nearly the same. The combination between Figure 1b and Table 1 shows that the gallium oxides also had a substantial reduction as the number of Al_2O_3 deposition cycles increased. This was mainly attributed to the role of Al_2O_3 in impeding oxygen and gallium diffusion.[23] The reduction of the Ga^{3+} oxides was also caused by the following reaction: $2Al(CH_3)_3 + Ga_2O_3 \rightarrow Al_2O_3 + 2Ga(CH_3)_3$. The Al precursor TMA depleted a portion of the Ga^{3+} oxides and produced the corresponding volatile substances.[22] The HGO/GaAs interface that was passivated by the 20 cycles Al_2O_3 still contained a certain number of Ga^{1+} oxides, which was in good agreement with the reported observation by Hinkle.[25]

Figure 2 shows the Hf 4f XPS core-level spectra for the S1, S2, and S3. All samples were decomposed into two contributions of Hf $4f_{5/2}$ and Hf $4f_{7/2}$ with a 1.67 eV spin-orbit doublet. The peaks of the S2 and the S3 samples shifted toward a binding energy, indicating that the Fermi level shifted toward a flat band condition occurs.[26]

Based on the evolution of the high resolution spectra of the As 3d, the Ga $2p_{3/2}$, and the Hf 4f, it could be concluded that the arsenic oxide, the gallium oxide, and the elemental arsenic between the HGO/GaAs interface was effectively suppressed and reduced when the 20 cycles Al_2O_3 passivation layer was introduced.

To improve the device scaling potential, in terms of a low gate leakage current, the high-k gate dielectrics require sufficient band offsets of over 1 eV for both the electron and the hole injection. The method proposed by Kraut[27] stated that the

Table 1. The peak area percentage of As^{1+}, As^{3+}, As^{5+} oxides and As° in As 3d core-level XPS spectra.

Samples	As° [area%]	As^{1+} [area%]	As^{3+} [area%]	As^{5+} [area%]
S1	9.02	6.17	13.05	6.83
S2	9.37	4.70	5.94	7.38
S3	3.48	2.86	2.86	7.48

Table 2. The peak area percentage of Ga^{1+}, Ga^{3+} oxides and Ga-S in Ga $2p_{3/2}$ core-level XPS spectra.

Samples	Ga-S [area%]	Ga^{1+} [area%]	Ga^{3+} [area%]
S1	9.98	13.91	8.99
S2	9.30	12.53	7.86
S3	9.82	7.47	2.93

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Table 3. Parameters of the MOS capacitors extracted from the *C*–*V* curves.

Samples	EOT [nm]	K	V_{fb} [V]	Q_{ox} [cm^{-2}]	ΔV_{fb} [V]	N_{bt} [cm^{-2}]	J [A cm^{-2}]
S1	1.60	34	1.47	-1.67×10^{13}	–0.37	4.98×10^{12}	2.17×10^{-3}
S2	1.51	39	1.30	-1.53×10^{13}	–0.14	2.00×10^{12}	5.90×10^{-4}
S3	1.52	42	1.12	-1.20×10^{13}	–0.05	7.00×10^{11}	3.57×10^{-4}
FGA@200 °C	1.47	43	1.08	-1.30×10^{13}	–0.05	7.33×10^{11}	1.55×10^{-5}
FGA@300 °C	1.43	44	0.64	-6.2×10^{12}	0.02	-3.02×10^{11}	5.87×10^{-6}
FGA@400 °C	1.43	45	0.79	-8.4×10^{12}	0.04	-6.00×10^{11}	6.57×10^{-4}

valence band alignment of the HGO films on the GaAs substrate without/with the Al_2O_3 passivation layer was detected. The valence-band spectra for the as-cleaned GaAs (0.35 eV) showed that the valence band offsets (ΔEv) between the GaAs substrates and the HGO thin films under various Al_2O_3 deposition cycles, as highlighted in **Figure 3**a, were found to be 2.02, 1.87, and 2.45 eV, respectively. The energy band gap of the sputtering-deposited HGO thin films were measured by UV–vis, as shown in Figure 3b. Combing the values of the energy band gap and the valance band offset, the conduction band offsets (ΔE_c) could be extracted. ΔE_c values of the S1, S2, and S3 were measured to be 2.29, 2.44, and 2.61 eV, respectively. **Figure 4** presents the schematic energy band alignment of the HGO/GaAs gate stack with and without the Al_2O_3 passivation layer. The band offset of the HGO/Al_2O_3/GaAs gate stacks were higher than 1 eV. There was an increase in the conduction band offset after the passivation layer was introduced, which aided the reduction of the leakage current.[28]

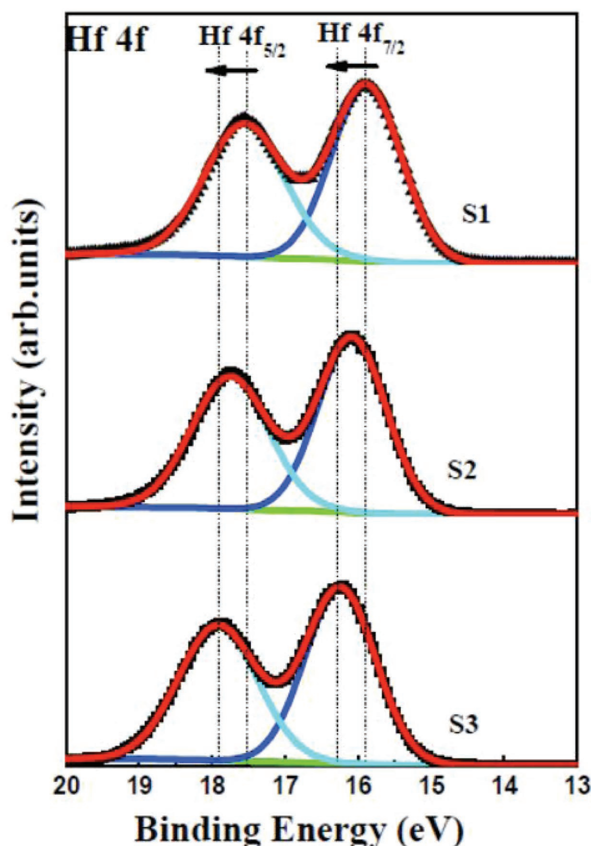

Figure 2. The Hf 4f core-level XPS spectra of S1, S2, and S3.

2.2. Electrical Properties Characterization

Figure 5a shows the typical high frequency *C*–*V* characteristics of S1, S2, and S3, which are swept from inversion to accumulation, and back. The high frequency (1 MHz)*C*–*V* curves could mitigate the impact of the MOS capacitor interface state and become the most frequently measured *C*–*V* curve.[29]The accumulation capacitances (C_{ox}) of S2 and S3 were higher than that of S1, even when the physical thickness of the two samples with an Al_2O_3passivation layer was larger than the sample without an Al_2O_3 thin layer. This was attributed to the blocking role of the Al_2O_3 passivation layer against the Ga/As outdiffusion and O in-diffusion. This suppressed the growth of the low-k interfacial layer on the GaAs surface. Except the interfacial layer thickness, the leakage current, the charges in the gate dielectrics, the different work functions between the metal and semiconductor (W_{ms}), and the interface state density were also the key factors that affected the performance of the MOS devices. The permittivity (*k*), the flat band voltage (V_{fb}), the hysteresis (ΔV_{fb}), the density of oxide charge (Q_{ox}), and the border trapped oxide charge density (N_{bt}) of the HGO gate dielectric were extracted from the *C*–*V* curves and listed in Table 3.The *k* value of the HGO thin films were 34, 39, 42 for samples S1, S2, and S3, respectively, which was similar to previous reported data.[30] The V_{fb} values for S1, S2, and S3 were 1.47, 1.30, and 1.12 V, respectively. The positive V_{fb} indicated the presence of negative oxide charges in the HGO thin films. This could be due to the introduction of electronegative sulfur ion following $(NH_4)_2S$ passivation. Besides, the upward energy band bending in the semiconductor space charge layer attributed to a positive value of W_{ms} required an extra positive voltage to appease the bent energy band. Table 3 and Figure 5a illustrate the tendency for the V_{fb} to decrease as the deposition cycles of Al_2O_3 passivation increased. The alteration of the oxygen vacancies simultaneously occurs with O in-diffusion. It has been reported that oxygen vacancies easily capture one or two electrons to form a center of negative charges.[31] This suggest that more oxygen vacancies in the gate dielectric, the larger positive flat voltage was required to keep the energy band at the semiconductor surface unbent. The XPS results demonstrated that the sample S3 with 20 cycles Al_2O_3 passivation layer had the ability to reach maximum retardation of oxygen diffusion. The oxygen vacancies

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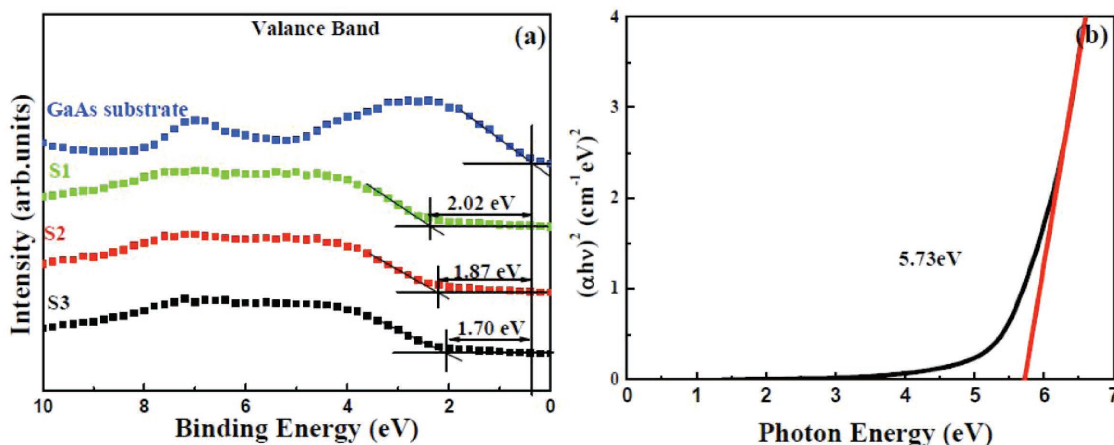

Figure 3. a) The VBM of HGO/Al_2O_3 and GaAs substrate of S1, S2, and S3; b) The determination of the band gap of HGO thin films grown on quartz substrates.

content of the gate dielectric in S3 sample was the smallest, which corresponded to the smallest flat band voltage value of 1.12 V. The values of Q_{ox} shown in Table 3, confirmed these results. Sample S3 possessed the least negative oxide charges, which could be due to the least amount of oxygen vacancies in the high-k thin films. The reduction of ΔV_{fb} as the Al_2O_3 deposition cycles increased were detected, originating from the lessening of the slow interface states density at or near the interface.[32] Compared to S1 and S2, the N_{bt} value of S3 had a significant reduction, which was closely related to the effective suppression of Ga and As diffusion. Figure 5a shows that the C–V characteristics of the three samples have similarities, including a larger "stretch-out," a smaller slope, and a marked intersection in the depletion region and unsaturated accumulation region, indicating a high interface-trap density and a slow interface states density. The capacitance in the inversion region continued to decrease, rather than stabilize, as the C–V curve become ideal, because the oxide leakage current caused the semiconductor surface to enter the deep depletion region. This resulted in a decrease in the MOS capacitance with increasing the width of the depletion region.[33] The leakage current density (J) as a function of the applied bias voltage (V) for S1, S2, and S3 are presented in Figure 5b. The specific values of J at 2 V are listed in Table 3. The overall larger leakage current of the three samples were observed, which confirmed the interpretation of the inversion MOS capacitance. The larger leakage current density was likely due to the high oxide charge and the trap charge. Compared to the sample S1 without Al_2O_3 passivation layer, the leakage current density of the samples with Al_2O_3 passivation layer had reduced an order of magnitude. This was caused by the large energy gap of the Al_2O_3 thin film and the increased conduction band offsets after the introduction of the passivation layer.

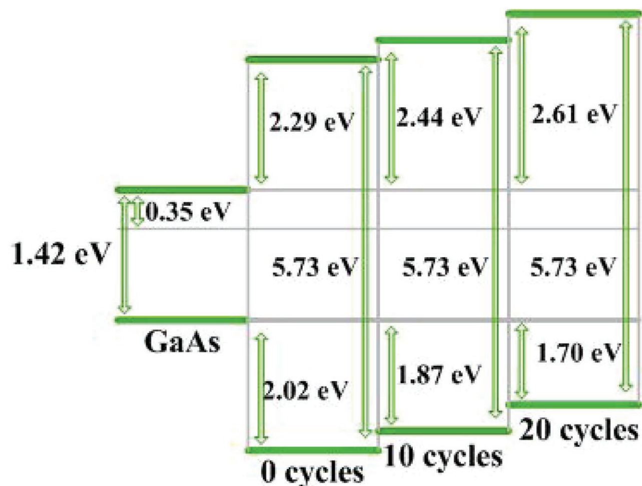

Figure 4. Schematic band diagram of the HGO films of S1, S2, and S3.

The HGO/GaAs gate stacks with 20 cycles Al_2O_3 passivation layer presents the improved interface quality with a suitable permittivity, the lowest oxide and trap charge density, and the lowest leakage current density. However, the overall electrical performance still requires optimization.

2.3. Electrical Performance Optimization by Forming Gas Annealing

The electrical properties of Al_2O_3passivation layer were considered when the forming gas annealing was performed to neutralize the trap charges and achieve better contact between the metal and the semiconductor. FGA was conducted on sample S3 at 200, 300, and 400 °C. **Figure 6** depicts the typical high-frequency (1 MHz) C–V characteristics of the HGO/Al_2O_3/GaAs MOS capacitors as a function of the FGA temperature. Note, the MOS capacitance of the 200 °C-annealed S3 sample at the inversion region was nearly identical, which suggested that the oxide leakage current was reduced after 200 °C FGA. The single C–V curve of the 200 °C-annealed sample is shown in inset of Figure 6. The slight intersection near the inversion region demonstrated the existence of the lower interface state at the HGO/GaAs interface. The leakage current density presented in Table 3 and Figure 6 decreased an order of magnitude due to the reduction of the interface states-assisted leakage current.[34] Especially, the 300 °C-annealed sample exhibited the

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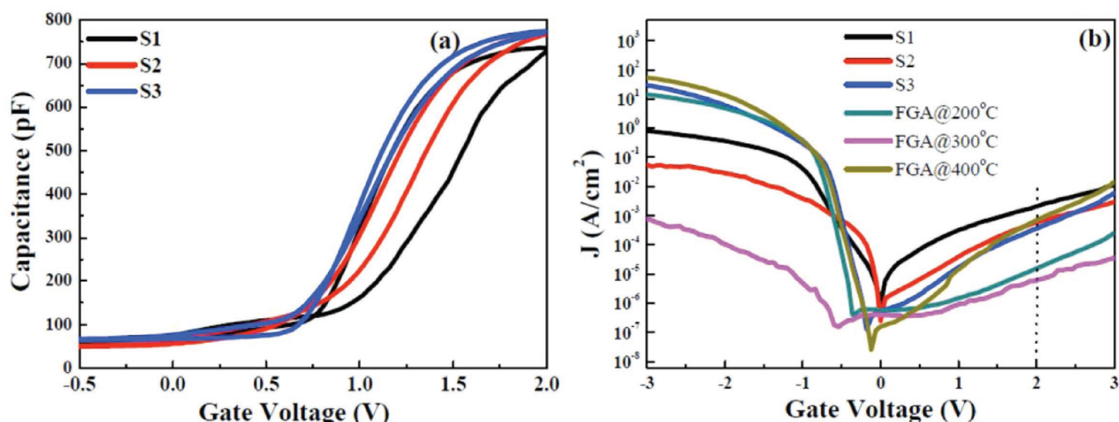

Figure 5. a) Capacitance–voltage (C–V) characteristics curves of S1, S2, and S3; b) Leakage current density–gate voltage (J–V) characteristics curves with different Al_2O_3 deposition cycles and forming gas annealing temperature.

best C–V behavior with smallest stretch-out, V_{fb} and ΔV_{fb} in the more steeper depletion regions and saturated accumulation. This was contributed to the reduction of the interface states, the oxide charge density, and the border trap charge density respectively, indicating the improved interface quality. The 300 °C-annealed sample with the smallest V_{fb} value of 0.64 V was affected by electronegative sulfur ion at the GaAs surface, the positive W_{ms}, and some of the movable charges in the gate dielectric. The remaining elemental As° at the GaAs surface was observed in the As 3d spectra of sample S3, which was thermally decomposed after the 300 °C annealing. The 300 °C-annealed sample with the leakage current density of 5.87×10^{-6} A cm^2 was lower than others, mainly owing to the reduction of the border trap-assisted and the interface states-assisted leakage current. When the annealing temperature increased to 400 °C, the V_{fb}, the ΔV_{fb}, and the leakage current density demonstrated an obvious increase, which could be due to the excessive temperatures resulting in interdiffusion between the metal and the film. This deteriorated the performance of the MOS devices.

A comprehensive understanding of the leakage current conduction mechanisms (CCMs) from the HGO thin film to the GaAs substrate or in reverse is important for the application of high performance MOS devices. The low temperature leakage current characteristic measurements were conducted to clarify the CCMs of the 300 °C-annealed Al/HGO/Al_2O_3/GaAs MOS capacitor, as shown in **Figure 7**. The values of the leakage current density of 77, 157, 237, and 300 K were 5.88×10^{-8}, 3.44×10^{-7}, 5.99×10^{-6}, and 5.87×10^{-6} A cm^{-2} at a gate voltage of 2 V, respectively. At the limit temperature of 77 K, the MOS capacitor had the lowest leakage current density. The leakage current density demonstrated an increasing trend as the temperature increased. This could be caused by the transformation of the CCMs at various temperatures. Possible CCMs for the 300 °C-annealed MOS capacitors included Direct tunneling (DT), Schottky emission (SE), and Poole–Frenkel emission (PF). It has been reported that the latter two belong to the thermionic emission, which is temperature dependent. The tunneling effect is virtually independent.[35] Both of them were confirmed by the experimental results. $E^{3/2}$ was proportional to $E\ln(J\ E^{-2})$

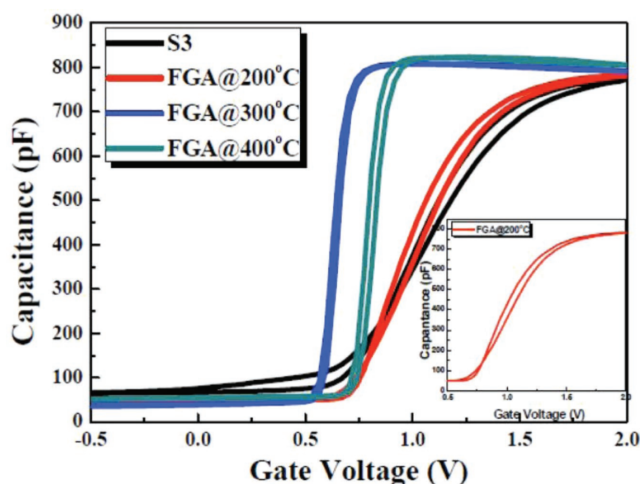

Figure 6. High-frequency (1 MHz) C–Vcharacteristics of HGO/Al_2O_3/GaAs MOS capacitors as a function of FGA temperature. The insert shows the single C–V curve of the 200 °C-annealed sample.

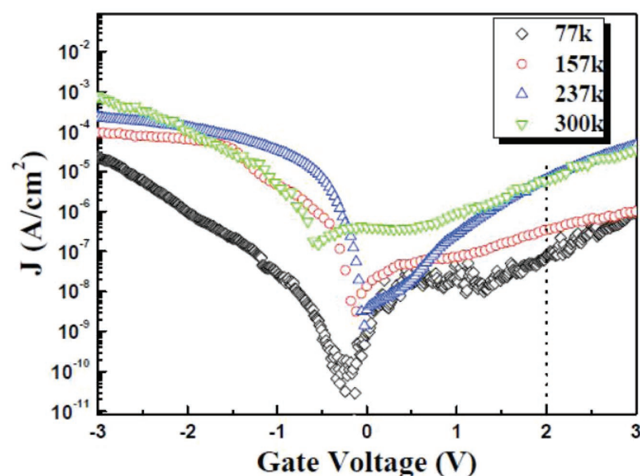

Figure 7. The low-temperature leakage current characteristic of the 300 °C-annealed Al/HGO/Al_2O_3/GaAs MOS capacitor.

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in the DT. $E^{1/2}$ was proportional to $\ln(J\ T^{-2})$ in the SE. For PF, $E^{1/2}$ was proportional to $\ln(J\ E^{-1})$.[36] The electric field E was the applied voltage minus the V_{fb}, divided by the HGO film thickness. **Figure 8**a,b depicts the plots of $E\ln(J\ E^{-2})$ versus $E^{3/2}$, $\ln(J\ T^{-2})$ versus $E^{1/2}$, and $\ln(J\ E^{-1})$ versus $E^{1/2}$ under substrate injection, respectively. Figure 8a shows the plots of $E\ln(J\ E^{-2})$ versus $E^{3/2}$ of the test temperatures yielded a good linear behavior at $E > 0.17$ MV cm^{-1}. This indicated that the CCM of directing tunneling existed in 77, 157, 237, and 300 K MOS capacitors. The plots of $\ln(J\ T^{-2})$ versus $E^{1/2}$ for 157, 237, and 300 K at $0.22 < E < 2.25$ MV cm^{-1} are presented in Figure 8b. At 77 k, there was no linear behavior for the above plot at any of the electric field ranges, indicating the transportation of the 77 K leakage current for MOS capacitor did not obey the Schottky emission. The optical dielectric constant ε_r and the refractive indexn ($\varepsilon_r = n^2$) was extracted from the slopes of the linear plots, which are displayed in Figure 8b. The n value of the HGO thin film at 157 K deviated from the value reported by He.[37] This implied that the Schottky emission was not the dominant CCM for the 157 K MOS capacitor. Figure 8b shows that the n values of 237 and 300 K MOS capacitors were consistent with He, indicating that the Schottky emission played an importance role in the transport leakage current. There was a good linear behavior found for the plots of $\ln(J\ E^{-1})$ versus $E^{1/2}$, as depicted in Figure 8c. The corresponding ε_{ox} values were estimated from the slopes of the linear plots, which were consistent with previous findings.[38–40] This suggested that the Poole–Frenkel emission was also a main CCM for 237 and 300 K MOS capacitors. The mainly CCM of 77 and 157 K MOS capacitors were primarily driven by direct tunneling. The Schottky emission played an important role in the 157 K MOS capacitors. The main CCMs of 237 and 300 K MOS capacitors were primarily direct tunneling, schottky emission, and Poole–Frenkel emissions. The 157 K MOS capacitor in Figure 7 possessed a higher leakage current density than the 77 K MOS capacitor, which was mainly ascribed to the dual function of tunneling effect and the thermionic effect. The continuous increase of the leakage current density of the 237 and the 300 K MOS capacitors was attributed to the triple effect of directing tunneling, Schottky emissions, and Poole–Frenkel emissions.

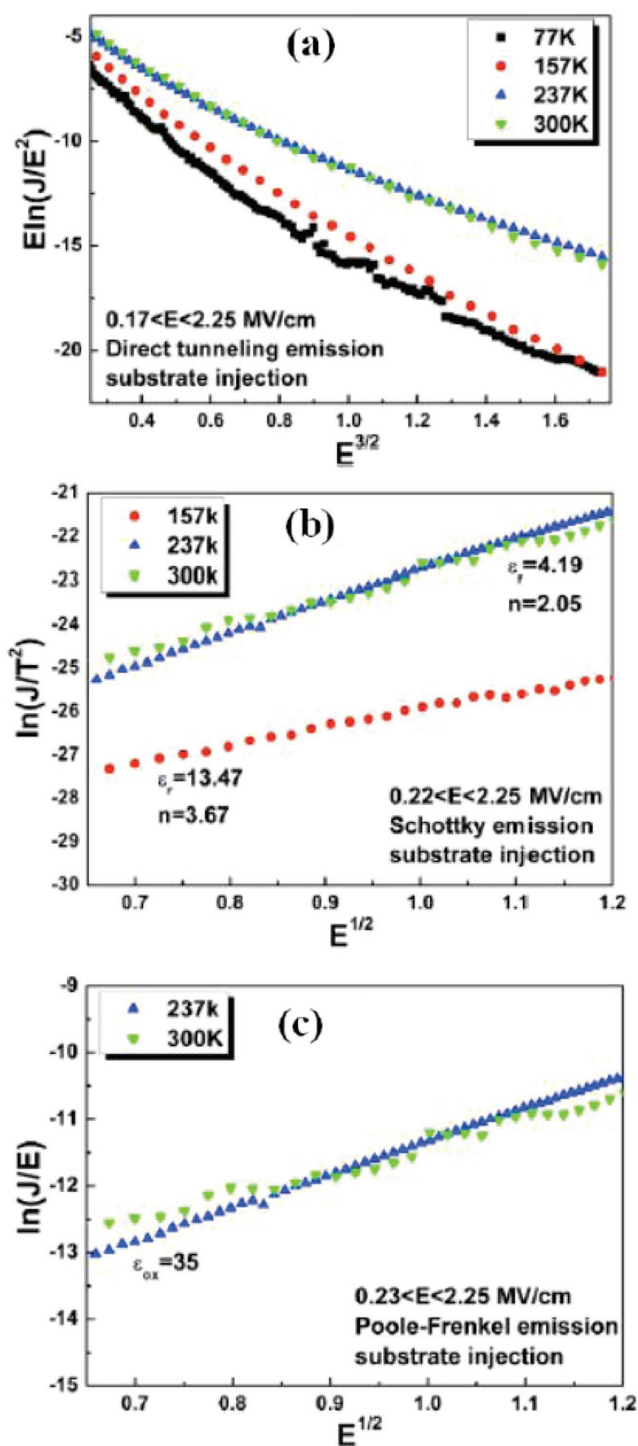

Figure 8. a) Characteristics of direct tunneling at various test temperatures under substrate injection; b) Characteristics of Schottky emission at various test temperatures under substrate injection; c) Characteristics of Poole–Frenkel emission at various teat temperatures under substrate injection.

3. Conclusions

Interface passivation was accomplished by introducing the Al_2O_3 thin layer prior to HGO deposition to suppress the interface species of the HGO/S-passivated GaAs gate stacks. The XPS results indicated that only the $(NH_4)_2S$ solution passivation was inadequate when removing the arsenic oxides, gallium oxides, and As°. After the 20 cycles Al_2O_3 thin layer was introduced onto the S-passivated GaAs wafer, the native oxides and elemental As° were removed except for As^{5+} oxides. The conduction band offset increased after the Al_2O_3 thin layer was introduced. These effects improved the C–V characteristics and reduced the leakage current density. There was a large amount of trap charges present in the high-k gate dielectrics. This led to the poor C–V behavior with larger "stretch-out," a smaller slope, and a marked intersection in the depletion region and the unsaturated accumulation region. The FGA was performed to neutralize those trap charges, to improve the electrical properties. According to high frequency (1 MHZ) C–V and J–V, the 300 °C-annealed MOS capacitor exhibited ideal C–V behavior with a moderate dielectric constant of 44, a smallest flat band voltage (V_{fb}) of 0.64 V,

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and a hysteresis (ΔV_{fb}) of 0.02 V. These values corresponded to the smallest oxide charge density (Q_{ox}) of -6.2×10^{12} cm^2, border trapped oxide charge density (N_{bt}) of -3.02×10^{11} cm^2, and the lowest leakage current density of 5.87×10^{-6} A cm^{-2}. The combination of the low temperature CCMs and the CCMs of the 300 °C-annealed MOS capacitor at room temperature (300 K) included directing tunneling, Schottky emissions, and Poole–Frenkel emissions. The combination of the introduced 20 cycles ALD-derived Al_2O_3 thin layer and the 300 °C forming gas annealing for the MOS capacitor effectively suppressed the regrowth of interface species and enhanced the performance of MOS devices, which will pave the way for the application of III-V-based MOSFETs.

4. Experimental Section

Commercially available Si-doped GaAs wafers (2×10^{18} cm^{-3}) were ultrasonically cleaned with acetone, ethanol, methanol, and isopropanol for 5 min, at room temperature, to remove organic and metallic impurities on the wafers. They were then rinse with deionized water for several times. The wafers were then immersed in a diluted HBr solution for 5 min to remove native oxides, and soaked in 20% $(NH_4)_2S$ for 20 min, at 50 °C to passivate the GaAs. The samples were dried with high purity nitrogen and the GaAs substrates were immediately loaded into an ALD vacuum chamber to deposit the Al_2O_3 passivation layer. Trimethylaluminium $[Al(CH_3)_3]$ and H_2O were used as the metal precursor and the oxidant, respectively. TMA was enclosed in a bubbler at room temperature and then transferred to the reaction chamber via high purity N_2. The ALD chamber temperature and the work pressure were 200 °C and 0.28 Torr, respectively. One Al_2O_3 growth cycle at 200 °C consisted of 0.02 s TMA pulse/8 s N_2 purge/0.02 s H_2O pulse/8 s N_2 purge at the growth rate of 0.12 nm per cycle. Three groups of samples with 0, 10, and 20 cycles of Al_2O_3 passivation (denoted as samples S1, S2, and S3) were deposited on the GaAs substrates. After deposition of Al_2O_3 layer, three samples groups were loaded into the vacuum chamber of a sputtering equipment together to deposit the HGO high-k gate dielectrics. The radio frequency reactive sputtering of the Gd-doped HfO_2 ceramic target was used to deposit the HGO thin films on the GaAs in an Ar ambient atmosphere at a flow rate of 20 SCCM (SCCM denotes cubic centimeter per minute at standard temperature and pressure). The radio frequency power, the working pressure, and the deposition temperature were fixed at 60 W, 0.6 Pa, and room temperature, respectively. 8 nm thick HGO films were measured by spectroscopy ellipsometer and prepared for XPS measurement to probe the interfacial chemical composition and the chemical bonding state between the GaAs substrate and the HGO thin film. The MOS capacitors were fabricated by deposited 15 nm HGO films on the GaAs substrate. A series of Al/HGO/Al_2O_3/n-GaAs/Al MOS capacitors were fabricated by sputtering an Al-top electrode with the area of 3.14×10^{-8} m^2 through a shadow mask and Al was deposited as the back electrode to decrease the contact resistance. FGA was performed at 200, 300, and 400 °C for 10 min on the MOS capacitors, which were marked as FGA@200 °C, FGA@300 °C, and FGA@400 °C, respectively. Figure S2 (Supporting Information) shows the details of the experimental procedure. The high-frequency (1 MHZ) *C–V* curves and the leakage current characteristics *J–V* were performed by a semiconductor device analyzer (Agilent B1500A) and a Cascade Probe Station. The electrical tests were subjected to short circuit and open circuit calibration before using the semiconductor device analyzer. After calibration, the *C–V* and *J–V* modules were chosen to quantify the electrical properties. The low temperature leakage current characteristics *J–V* were conducted by a Lakeshore Probe Station. The vacuum probe station chamber was filled with liquid nitrogen to achieve the lower temperature (77–300 K). The operating procedures of the probe station were identical to the Cascade Probe Station.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

electrical properties, forming gas annealing, high-k gate dielectrics, interface chemistry, metal-oxide-semiconductor capacitors

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