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Progress in the development of the EAST timing synchronization system upgrade based on precision time protocol

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ABSTRACT

The timing synchronization system (TSS) plays an important role in the experiments of the Experimental Advanced Superconducting Tokamak (EAST). The purpose of this system is to synchronize each subsystem of EAST according to the reference clock and delay trigger signal, and ensuring stable operation of the EAST fusion device. A prototype TSS module based on precision time protocol (PTP) has been developed using the PXI bus standard and FPGA devices. This new TSS can provide reference clock signals with frequency of up to 50 MHz with isolation fan-out devices. The maximum trigger skewing between different nodes is less than 10 ns. This new TSS is more expandable and suitable for the synchronization and timing control of the EAST fusion experiment. It has been in steady operation since the 2016 EAST experimental campaign. This paper concentrates on the modifications of the TSS, the details about the system architecture and test results will be described in this manuscript.

1. Introduction

The Experimental Advanced Superconducting Tokamak (EAST) has fully superconducting tokamak with a non-circle cross-section of the vacuum vessel and the active cooling plasma-facing components [1]. This key national project consists of many subsystems which are spread out over relatively large distances that need to be synchronized by a synchronization control mechanism to maintain the stable operation of the fusion device.

The former distributed synchronization and timing system (DSTS) on the EAST was based on a set of synchronized optical network which was made up of several pairs of multi-mode fibers. All the nodes distributed in experimental area were connected by these same-length fibers [2]. The accuracy of the system synchronization depended on the difference in fiber lengths among timing nodes, and each node's delay time hinged on the route of the fiber. Therefore it's difficult for maintainers to add new timing nodes to meet the ever increasing demands of the experiments. The motivation for this system upgrade is to set up a stable timing synchronization system (TSS) that is also easy to expand, and convenient to maintain. The new system should provide reference clock signals with frequency of up to 50 MHz, and the synchronization accuracy between different nodes should be in sub-microsecond range.

At present, the most accurate way to synchronize the distributed data acquisition systems is to use the precision time protocol (PTP) IEEE 1588 2008 standard. The protocol is adopted by the EAST CODAC (Control, Data Access and Communication) system to implement the upgraded TSS prototype node. All the nodes with PTP in different places have access to the timing network by normal Ethernet cable, and the timing module on each chassis is synchronized with other IEEE 1588 devices on the network. This paper is organized as follows: the knowledge of PTP is described in Section 2; the structure and the realization of the TSS are presented in Section 3; the application results are shown in Section 4; and finally, the summary is given in Section 5.

2. IEEE 1588 technology overview

IEEE 1588 enables heterogeneous systems that include clocks of various inherent precision, resolution, and stability to synchronize to a grandmaster clock. It supports system-wide synchronization accuracy in the sub-microsecond range with minimal network and local clock computing resources. The protocol has features to address applications where redundancy and security are a requirement [3]. IEEE 1588 defines a special "clock synchronization" procedure [4]. The message exchange of PTP is illustrated in Fig. 1.

The master clock initiates offset correction using "sync" and "follow-up" messages. When the master sends a sync message, the slave uses its local clock to timestamp the arrival of the sync message and compares it to the actual sync transmission timestamp in the master clock's follow-up message. The difference between the two timestamps represents the offset of the slave plus the message transmission delay.

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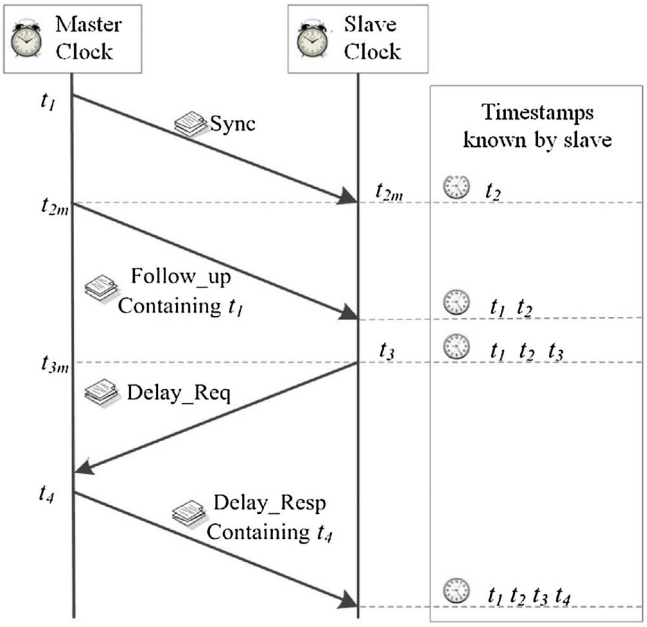


Fig. 1. Messages exchange of PTP.

The slave clock then adjusts the local clock by this difference. To correct for the message transmission delay, the slave uses a second set of sync and follow-up messages with its corrected clock to calculate the master-to-slave delay. The second set of messages is necessary to account for variations in network delays. The slave then timestamps the sending of a delay request message. The master clock timestamps the arrival of the delay request message. It then sends a delay response message with the delay request arrival timestamp. The difference between the time-stamps is the slave-to-master delay. The slave averages the two directional delays and then adjusts the clock by the delay to synchronize the two clocks. Because the master and slave clocks drift independently, periodically repeating offset correction and delay correction keeps the clocks synchronized [5]. The slave clock can get the offset and delay from Eqs. (1) and (2).

$$offset = \frac{t_2 - t_1 - t_4 + t_3}{2} = \frac{(t_2 + t_3) - (t_4 + t_1)}{2} \quad (1)$$

Table 1
The trigger signal properties and functions.

Property	Function
Node Number	Queries and retrievals signal in a small range
Channel Number	Describes the signal location in each node
Signal Name	Describes the main function of each channel
Delay Time	Sets delay time for each trigger channel with 1 ms step
Pulse Width	Sets pulse width for each channel with 1 ms step
Signal Polarity	Sets the signal polarity, such as positive or negative
Channel Enable	Offers the option of enabling trigger
Belonging Subsystem	Describes the destination subsystem that receives the signal

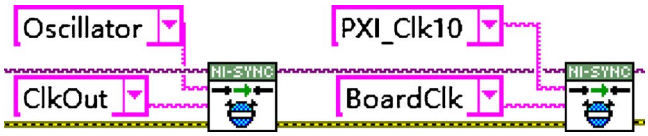


Fig. 3. Block diagram of routing.

$$MSDelay = \frac{t_2 - t_1 + t_4 - t_3}{2} = \frac{(t_2 + t_4) - (t_1 + t_3)}{2} \quad (2)$$

IEEE 1588 message timestamp is the basic factor for IEEE 1588 technology. Ethernet transceiver IC and PHY chips which support timestamp mark are often used to develop in-house devices. In this prototype system, NI PXI-6683 series synchronization boards are used to exchange the PTP messages.

3. System architecture

The upgraded TSS inherits the former console host and database server, optimizes the isolation fan-out modules, and constructs a set of PTP network. The structure of the TSS with two slave nodes is illustrated in detail in Fig. 2.

The master node (MN) and two slave nodes (SNs) are all based on the PXI platform. The MN and SNs are connected by the PTP network. When a system is initialized, the node which receives the GPS signal is defined as the master node as mandated by the software process. All other clocks become slaves and synchronize their clocks with the master. Each node's reference clock is routed to the chassis' backplane, so that all the nodes share the same synchronization time base. The

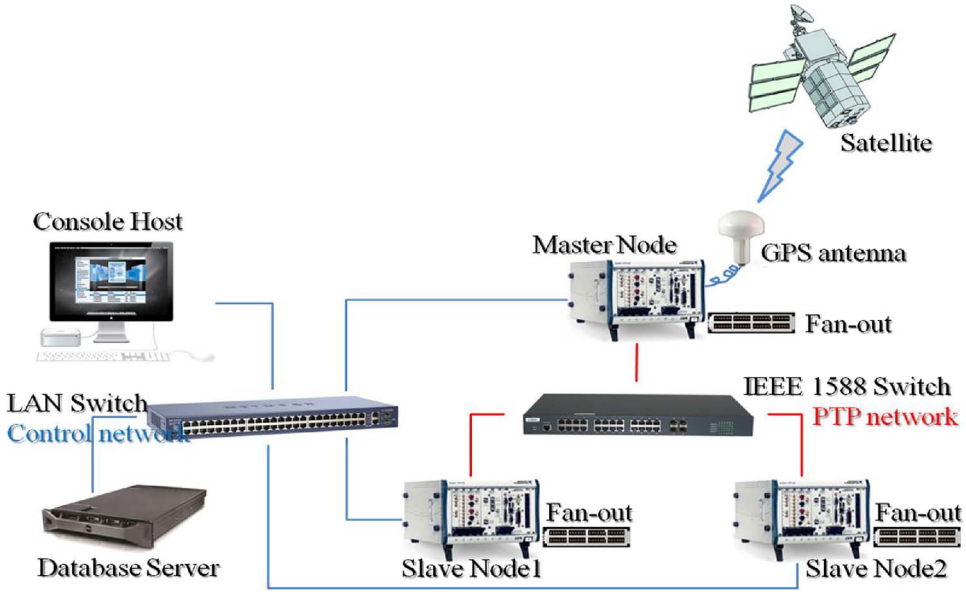


Fig. 2. Structure of upgraded TSS.

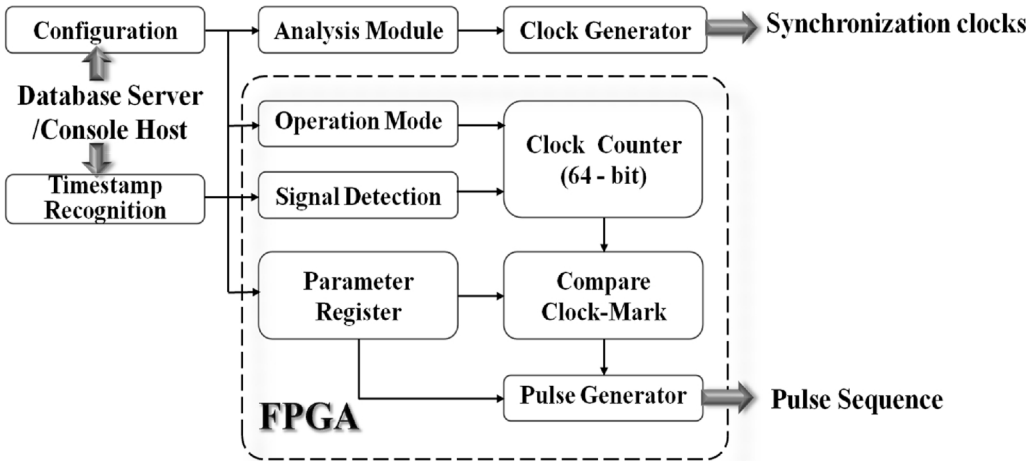


Fig. 4. Logic modules of the PXI node.

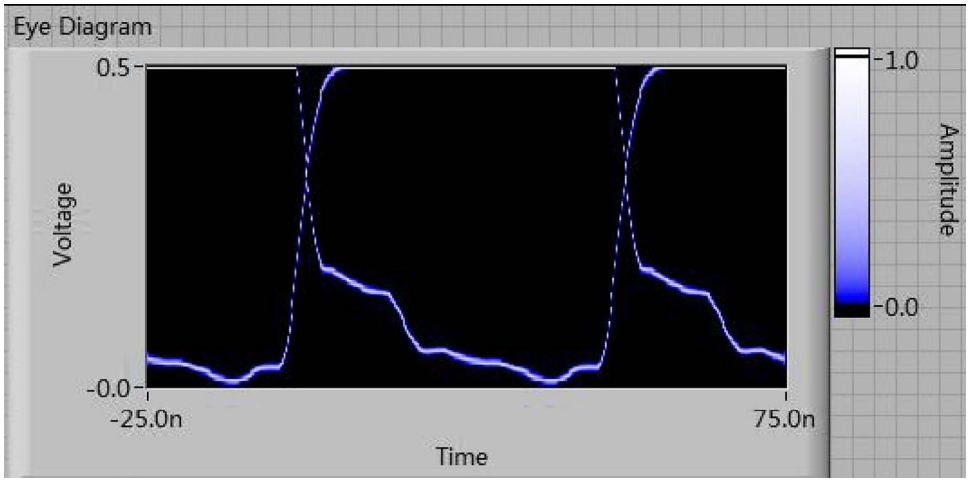


Fig. 5. Eye diagram of 10 MHz synchronization clock.

high-precision counter module in TSS node outputs reference clock. The FPGA module is used to generate the triggers. On the console host, set by the operator, parameters of each node and future time events (FTE) are transmitted to the PXI nodes and database server through the gigabit EAST control network [6]. The FTE includes the subsystem event information code and the future absolute time. The nodes receive the messages, decode the information and start to work at the pre-set absolute time. Operator activates a new shot, the central control system will starts to countdown. The physical experiment steps into DISCHARGE phase when the countdown timer reaches zero. During the DISCHARGR phase, the TTS system scans the status of interlock system. Once an event emerged (such as the subsystem has abnormal condition), the TTS stops the discharge schedule.

3.1. Console host

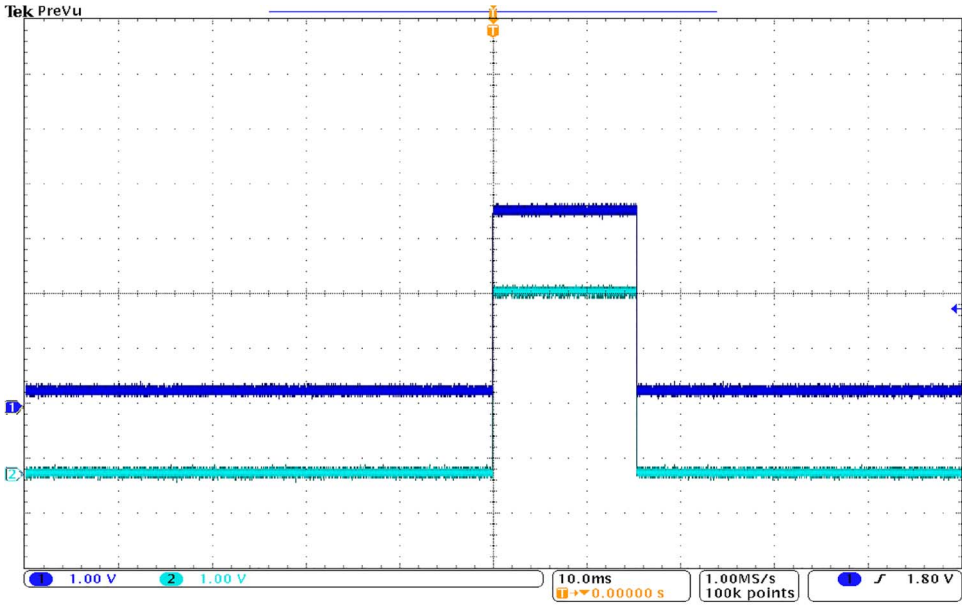
The TSS console host is integrated into the latest edition of the EAST central control system GUI. The operator can set the channel characteristics, such as signal name, delay time, pulse width, signal polarity, *etc*. The TSS node, channel number, and signal belonging subsystem are used as the indices with which to query the trigger information. The main signal properties and functions are summarized in Table 1.

3.2. Database server

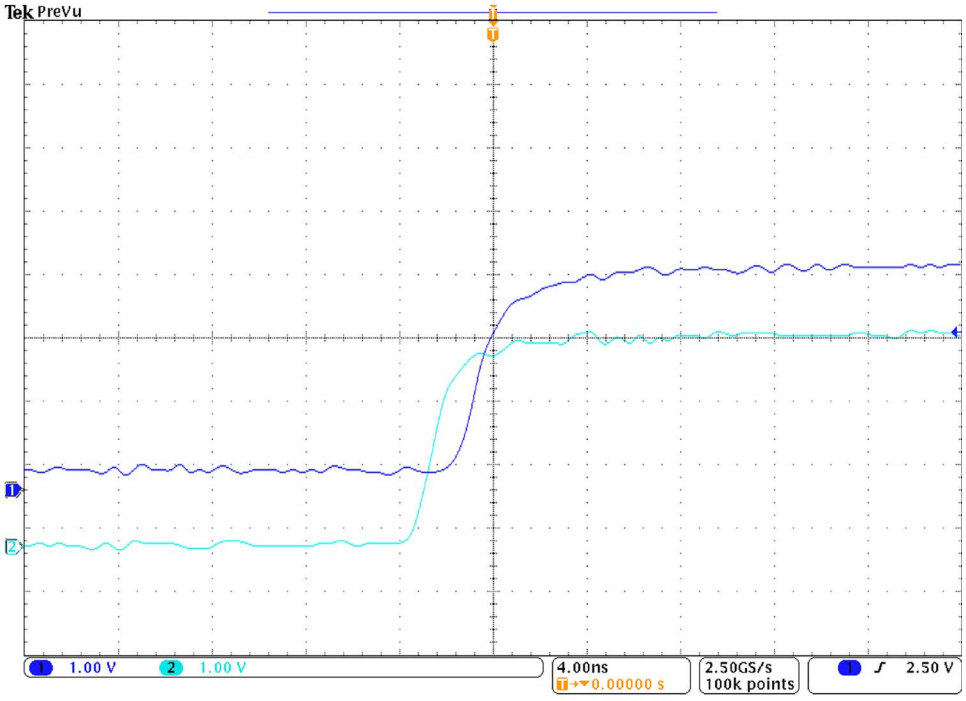
The database server includes two parts for redundancy: MySQL in Linux and Microsoft Access in Windows. The main server, MySQL database, is an ideal choice to deal with data concurrency and stability on the Linux platform as it provides multi-thread and multi-user access mechanisms [7]. The Access database on local disk is easier to manage with friendlier graphical interface. At the end of each shot experiment, the latest shot information with the complete trigger parameters is stored in both MySQL and Access. The shot number and channel belonging subsystem in the database table are optional items to recall archiving information for the next shot.

3.3. TSS network

Network performance is a critical factor for the distributed synchronization system. The network includes two parts: control network and PTP network. The control network, using a normal network switch, connects the computer, database server and PXI controller by Ethernet cable. Channel parameters and future time events (FTE) information are transferred from the console host to each node. The PTP network is made up of a switch and several timing modules. All the devices in the network should be supported by the IEEE 1588 protocol. The model of the switch is Hirschmann MAR1040 which is widely used in ITER, and the professional facility brings significantly accuracy. The device which receives the time from a satellite through the GPS antenna is defined as master node, the others nodes keep the time synchronized with the master node through Ethernet port.



(a) timescale is set to 10 ms/div, sampling rate is 1 MS/s,



(b) timescale is set to 4 ns/div, sampling rate is 2.5 GS/s

Fig. 6. Test results of the delayed trigger signals.

3.4. TSS PXI node

The nodes including master node (MN) and slave nodes (SNs) are based on the PXI platform with the same configuration. Each node is comprised of: (i) an 8-slot chassis featuring a high-bandwidth backplane with PXI capability in every slot; (ii) a Commercial Off-The-Shelf (COTS) controller equipped with an Intel Core i7 processors and 4G DDR3RAM; (iii) a high-precision counter/timer module PXI-6608 features a 10 MHz oven-controlled crystal oscillator (OCXO); (iv) a multifunction reconfigurable I/O module PXI-7842R with a Virtex-5 LX50 FPGA on board [8]; (v) a PXI-6683H timing and synchronization module to synchronize the PXI systems using GPS or IEEE 1588.

The PXI-6683H timing module on each chassis is synchronized with other IEEE 1588 devices through the PTP network. Since the PXI-6683H is a hybrid card and does not fit in the timing slot of the chassis, it cannot override the chassis' backplane directly. By using the niSync connect clock terminals VI, the on-board oscillator is routed to the PXI-6683H CLKOUT channel and the backplane clock is routed to the board clock. The block diagram is illustrated in Fig. 3. By connecting the CLKOUT terminal of the PXI-6683H to the 10 MHz Ref-In channel of the

chassis, the PXI 10 MHz backplane clock (PXI_Clk10) on the chassis is synchronized to the IEEE 1588 reference time.

The main software RT VI in PXI controller is encapsulated in various application modules and the block diagram is presented in Fig. 4.

All the modules are named after their functions. The RT VI receives the latest FTE from console host or database server. The configuration module decodes the information in FTE, and transfers the parameters to the next modules. The frequency parameters are required by analysis module to calculate the duty cycle of reference clocks. Operation mode and pre-set trigger parameters are used to configure the FPGA logic block pins. Upon arriving the absolute time in FTE, clock counters begin to count the tick, compare the current time and the pre-defined time. When the comparison result is equal, the pulse generator module outputs the pulse sequence.

3.5. Isolation and drive module

The isolation and drive module is a custom device which is used to remove ground loops among the different subsystems. All the digital signals and analog signals are isolated by multiple mode optical fiber links. Each output channel is driven by an optic fiber transmitter, Agilent HFBR-1414TZ. For the trigger signals, an Agilent HFBR-2412TZ receiver is used for solution of DC to 5 MBd TTL data at distances between 0 and 1700 m [9]. A kind of VFC (Voltage Frequency Converter) chip AD652 is used for transmitting analogue signals.

4. System output test results

The eye diagram is used to observe the effect of inter-symbol interference and noise, which can be used to estimate the extent of the system. A 10 MHz synchronization clock generated by the clock generator is sampled at a rate of 12 GS/s by an NI digitizer. The program achieves the eye diagram as shown in Fig. 5.

The synchronization of the trigger output is the most critical index for the TSS. Two trigger signals generated by the master node and slave node are set with the same characteristics: delay time = 0, pulse width = 15 ms, signal polarity: Positive, Channel enable = enabled. Fig. 6 shows the test results on a signal oscilloscope.

In Fig. 6(a), the timescale is set to 10 ms/div and the sampling rate is 1 MS/s. The pulse-widths of the two signals are 15 ms, which equals the pulse-widths of the preset pulses. In Fig. 6(b), the timescale is set to 4 ns/div and the sampling rate is 2.5 GS/s. The rising edges between the two positive signals are less than 10 ns. This shows that the trigger signals with the same preset parameters in two different nodes have good time synchronization and the maximum skewing is less than 10 ns.

5. Conclusions

Based on precision time protocol, a new TSS has been developed by using PXI devices. It aims at building a synchronization system that is easily expanded and conveniently maintained. The PXI node which receives the GPS signal is defined as the master node. The others IEEE 1588 timing modules in the PTP network are connected with standard Ethernet cables. The new TSS can provide the reference clock signal with a frequency up to 50 MHz with isolation fan-out devices. The maximum trigger skewing between different nodes is less than 10 ns. Although the prototype system is expansive than the former DSTS, the new TSS is more expandable and suitable for the synchronization and timing control of the EAST fusion experiment. The next step is to custom some devices by using ARM, and some of the progresses will be released in the future.

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