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High-performance Ge-on-Si photodetectors

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The past decade has seen rapid progress in research into high-performance Ge-on-Si photodetectors. Owing to their excellent optoelectronic properties, which include high responsivity from visible to near-infrared wavelengths, high bandwidths and compatibility with silicon complementary metal–oxide–semiconductor circuits, these devices can be monolithically integrated with silicon-based read-out circuits for applications such as high-performance photonic data links and infrared imaging at low cost and low power consumption. This Review summarizes the major developments in Ge-on-Si photodetectors, including epitaxial growth and strain engineering, free-space and waveguide-integrated devices, as well as recent progress in Ge-on-Si avalanche photodetectors.

For many years, high-quality Germanium (Ge) crystals have been used as the primary material for highly sensitive near-infrared detectors. Such detectors are usually cooled to around 77 K to reduce dark currents, making them expensive and of limited use, particularly for spectroscopy. However, within the past ten years, the use of Ge in detector applications has changed dramatically. This development was triggered by the ability to grow Ge epitaxially on silicon (Si). Rather than using single-crystal bulk Ge, the use of Si as a substrate not only reduced device cost but also enabled completely new applications for Ge in optical communications, which until then had typically been covered by compound semiconductors such as InGaAs.

The epitaxial growth of Ge on Si is difficult because of the 4.2% lattice mismatch between the two elements. In the 1990s, the first attempts were made to epitaxially grow Ge on Si at reasonably low dislocation densities, primarily motivated by the higher mobilities for electrons and holes in Ge than in Si. This Review first describes the techniques that eventually yielded high-quality Ge-on-Si devices. Initially this progress was used to develop free-space Ge detectors with responsivities and speeds comparable to group III–V semiconductor detectors. The development of the free-space Ge detector, and the following evolution to the waveguide-integrated Ge detector, is discussed. This evolution not only enabled electronic–photonic integration on silicon but also achieved higher performance by eliminating the trade-off between bandwidth and quantum efficiency. Different coupling schemes and their corresponding performances are also reviewed. Finally, the recent progress of Ge-based avalanche photodetectors is discussed, as these important devices are currently competing with group III–V avalanche photodetectors for a market share in optical communications.

Choice of materials

Growth of high-quality Ge epitaxial films on Si. The greatest challenge for high-quality Ge epitaxy on Si is the 4.2% lattice mismatch between the two materials. This mismatch causes two serious issues: high surface roughness resulting from the Stransky–Krastanov growth, and a high density of threading dislocations in the Ge epitaxial layer. High surface roughness hinders the process of integrating Ge devices with Si electronics because complementary metal–oxide–semiconductor (CMOS) devices require planar processing, whereas a high density of threading dislocations severely affects the performance of Ge devices because of the recombination centres that are introduced along these dislocations.

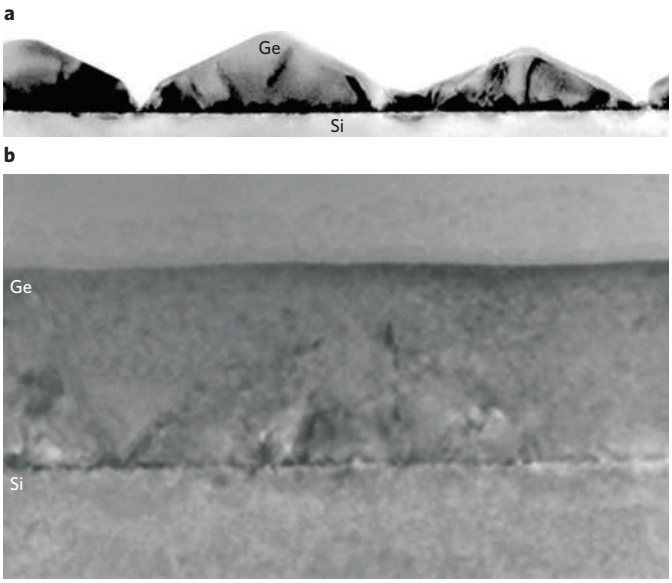

Figure 1 | Transmission electron microscope cross-sections of Ge-on-Si layers for Ge epitaxial growth at different temperatures. a, Stransky–Krastanov growth of Ge-on-Si at 550 °C in an ultrahigh vacuum CVD reactor. **b**, Ge-on-Si grown at 335 °C in an ultrahigh vacuum CVD reactor. The thickness of the Ge layer shown here is 60 nm.

The first successful approach for growing high-quality epitaxial Ge layers on Si was reported in a forward-looking paper by Luryi *et al.* in 1984[1]. In this study, a graded SiGe buffer layer, grown in a molecular beam epitaxy chamber, was used to reduce the threading dislocation density in the Ge layer. This method was later improved by Fitzgerald *et al.* using optimized SiGe graded buffer layers[2–5]. A low grading rate of ~10% Ge per micrometre was adopted to minimize dislocation nucleation rates. Choosing adequate growth temperatures for different SiGe compositions gave a high dislocation glide velocity but slow dislocation nucleation kinetics, allowing the film to relax mainly by gliding existing threading dislocations instead of generating additional dislocations. At 50% Ge composition, an *ex situ* chemical mechanical polishing step was used to remove crosshatch surface roughness and greatly reduce the dislocation pile-up formation that hinders dislocation gliding. For SiGe growth with Ge content of more than 50%, the growth

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temperature was gradually decreased to accommodate the reduction in the yield strength of the material and to prevent nucleation of dislocations. This approach was used to successfully demonstrate Ge films with threading dislocations of $<2 \times 10^6$ cm^{-2}.

High-quality epitaxial Ge-on-Si growth has also been achieved through adequate direct Ge growth without using SiGe buffers layers. In this case, a two-step Ge growth technique is used to prevent islanding during the ultrahigh vacuum chemical vapour deposition (CVD) process, with subsequent annealing to significantly decrease the threading dislocation density[6–8]. In the initial growth step, a thin epitaxial Ge buffer layer of 30–60 nm is directly grown on Si at 320–360 °C. At such low growth temperatures, the low surface diffusivity of Ge kinetically suppresses the islanding of Ge. The growth temperature in the main growth step is increased to >600 °C to achieve higher growth rates and better crystal quality. If the low-temperature buffer layer is thick enough (>30 nm), the Ge atoms are no longer influenced by the Ge/Si lattice mismatch and so homoepitaxial Ge growth results. The film therefore remains flat even at elevated growth temperatures, and fully planar growth is achieved. Figure 1 shows cross-sectional transmission electron microscope images of Ge-on-Si grown by the single- (Fig. 1a) and two-step (Fig. 1b) growth methods. The threading dislocation density of the as-grown (that is, without post-growth annealing) film is typically of the order of 10^8–10^9 cm^{-2}. Adequate post-growth annealing at >750 °C can reduce the threading dislocation density by up to two orders of magnitude[8]. Koester *et al.* have extended this two-step approach by demonstrating growth of Ge on an ultrathin silicon-on-insulator surface[9,10]. In this case, however, the thermal annealing process for reducing threading dislocations is compromised by interdiffusion between Si and Ge layers, which is possibly related to the instability of the ultrathin silicon-on-insulator layer.

Another direct Ge growth approach uses H_2 annealing at around 825 °C instead of a two-step growth process to reduce the surface roughness and threading dislocation density of epitaxial Ge films[11,12]. The enhanced atomic mobility under H_2 annealing was proposed to be the major mechanism for the reduction in surface roughness and defect density.

Different approaches have been developed in recent years to achieve high-quality Ge epitaxy on Si at lower temperatures. For example, the thin Ge buffer layer was altered by combining thin SiGe buffer layers (<<1 μm) with the two-step Ge growth approach[13,14]. A low threading dislocation density of $<7 \times 10^6$ cm^{-2} was reported. Very recently, low-energy plasma-enhanced CVD has been developed to achieve high-quality Ge at a lower thermal budget than ultrahigh vacuum or low-pressure CVD[15].

Tensile-strained Ge-on-Si. Strain has a significant effect on the band structure and optoelectronic properties of semiconductor epitaxial layers. It is therefore important to understand and engineer the strain in epitaxial films for optoelectronic applications. The effect of tensile strain on the band structure of Ge at 300 K is shown in Fig. 2. Relaxed Ge has an indirect gap of 0.664 V at the L valley (in <111> directions), and a direct gap of 0.800 eV at the Γ valley ($k = 0$). When biaxial tensile stress is applied, both the direct and indirect gaps shrink, but the direct gap shrinks faster. Therefore, Ge transforms from an indirect to a direct gap material with the increase of tensile strain, and its optoelectronic properties are greatly enhanced accordingly. Compressive strain, on the other hand, increases the difference between the direct and indirect gaps of Ge, which is detrimental to its optoelectronic properties. It is therefore desirable to have tensile-strained Ge instead of compressive-strained Ge for high-performance optoelectronic devices on Si.

Because the lattice constant of Ge is greater than that of Si, very thin epitaxial Ge layers (tens of nanometres) and Ge nanostructures on Si are usually compressively strained. However, because

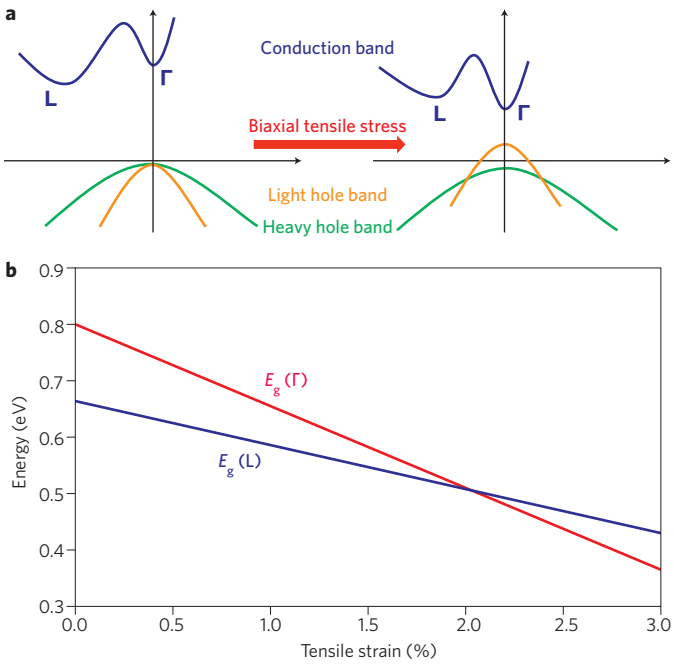

Figure 2 | The effect of tensile strain on the band structure of Ge. **a**, Schematic of how the band diagram changes as biaxial tensile strain is applied. **b**, Plot of the bandgap energies for the Γ (E_g(Γ)) and L (E_g(L)) bands as a function of tensile strain.

the critical thickness for two-dimensional coherent growth of Ge on Si without relaxation is usually only around three monolayers (~0.814 nm) because of the significant lattice mismatch[16,17], a Ge layer thicker than 200 nm can nearly completely relax at growth temperatures above 600 °C. When cooled to room temperature, tensile strain — instead of compressive strain — can accumulate in the Ge layers because of the larger thermal expansion coefficient of Ge compared with Si. This is usually the case for epitaxial Ge films fabricated by the two-step growth for optoelectronic applications, as the Ge film thickness required for a strong interaction with near-infrared light is usually >200 nm, and the second step of growth is usually performed at temperatures above 600 °C (refs 18–20). A thermally induced tensile strain of 0.25% has been achieved using this approach. In recent years, relaxed GeSn buffer layers on Si have been developed as a lattice template for tensile strained Ge (refs 21,22) to further enhance the tensile strain in Ge. This approach has so far achieved tensile strains of up to 0.68% (ref. 23).

Selective growth of Ge on Si. For the integration of Ge-on-Si devices into Si-based circuits, it is highly desirable to grow Ge selectively within designated regions on the Si substrate. Selected Ge growth will aid the process flow and allow transistors to be fabricated before the Ge processing stage. Furthermore, selective growth reduces the threading dislocation density if the selective growth region is small enough (<40 μm), as dislocations can glide to the edge of the mesas and annihilate[8,24]. In recent years, selective growth has also been applied to epitaxial necking and lateral overgrowth for achieving high-quality Ge-on-Si growth[25,26]. The selective growth of SiGe and Si with gas precursors has been developed since the mid-1980s[27]. Selective growths are usually achieved by using a dielectric mask layer such as SiO_2 or Si_3N_4. Openings are etched through the dielectric layer and reach the surface of the single-crystal Si layer; Ge can be selectively grown in these windows at adequate growth rates. An SiO_2 mask is used because the reaction between the SiO_2 mask layer and GeH_4 and/or Ge atoms is thought to be what forms volatile GeO

under high vacuum and prevents the nucleation of poly-Ge on SiO_2 (refs 28,29). To maintain the selective growth, Ge must be deposited at a slower rate than the desorption rate of Ge-related volatile species; otherwise Ge islands begin to nucleate on the dielectric layer and so the selectivity is lost.

Figure 3a shows a three-dimensional atomic force microscope image of a selectively grown Ge mesa. The mesa is faceted, with the (111) and (113) facets dominating when the oxide openings are aligned to a <011> direction. Similar orientation-dependent faceting is also observed in the case of a selective Si homoepitaxy.

The selective growth of Ge provides new methods of defining Ge photonic structures on Si. By completely filling the oxide windows and suppressing faceting, Ge growth can be included in a planar CMOS process flow, as shown in Fig. 3b.

Normal-incidence photodetectors

The first platform for high-performance Ge-on-Si photodetectors was normal-incidence detectors for free-space or fibre-optic coupling. This section reviews the advances and shortcomings of normal-incidence detectors, including the design parameters for high-speed detectors, the graded-index buffer approach, Ge-on-insulator detectors and Ge-on-Si detectors.

Historically, although Ge did have the distinct advantage of ease of integration with Si over InGaAs for light detection in the telecommunications wavelength range of 1,300–1,600 nm, performance of these Ge detectors needed to be as good as or better than the competing group III–V detectors. High responsivities, high bandwidths and low dark currents were therefore mandatory.

Thermionic emission limits the dark current density in Ge photodiodes to ~10^{-2} mA cm^{-2} at room temperature, which is around two orders of magnitude higher than competing InGaAs semiconductor photodetectors. A dark current density of 0.15 mA cm^{-2} at a reverse bias of −1 V is among the lowest reported for Ge-on-Si devices[4], and this is due to the low dislocation densities for Ge photodiodes fabricated on optimized SiGe graded buffer layers. Despite the high Ge quality and low dark currents present in this study, the thin depletion region of 0.3 μm resulted in low responsivity. In view of the integration with Si CMOS circuits, the thick SiGe buffer layer (~10 μm) required to achieve high-quality Ge makes integration difficult.

For a long time it was thought that a high-quality Ge detector would require near-perfect crystal quality. It was also suspected that dislocations — threading dislocations in particular — would increase dark current and therefore degrade device quality. Using thin Ge[30–39] or SiGe[13,40,41] buffer layers therefore seemed counterintuitive for achieving high-performance devices, as their threading dislocation densities are ~10 times higher than in optimized SiGe graded buffer layers. However, Ge photodetectors based on thin buffers and p-i-n (p-type/intrinsic/n-type layers) structures were found to exhibit a significant built-in electric field of several kV cm^{-1} inside the intrinsic Ge layer, making the carrier collection dependent not on carrier diffusion but rather on carrier drift[20,33]. This difference is significant because a dependency on carrier diffusion results in a relatively long transit time and significant carrier recombination at dislocations or point defects, thereby reducing the collection efficiency of the detector. Carrier drift, on the other hand, ignores recombination centres that have recombination times larger than the time it takes for a carrier to drift to the electrodes. For thin Ge layers of the order of 1–2 μm, a strong enough built-in electric field for carrier collection can easily overcome recombination processes at lattice defects. The built-in electric field was therefore the enabler for thin, high-quality Ge-on-Si photodetectors. The first Ge photodetectors with a thin buffer and reduced threading dislocation density through post-growth annealing showed remarkable responsivities over a large wavelength range[30], with an internal quantum

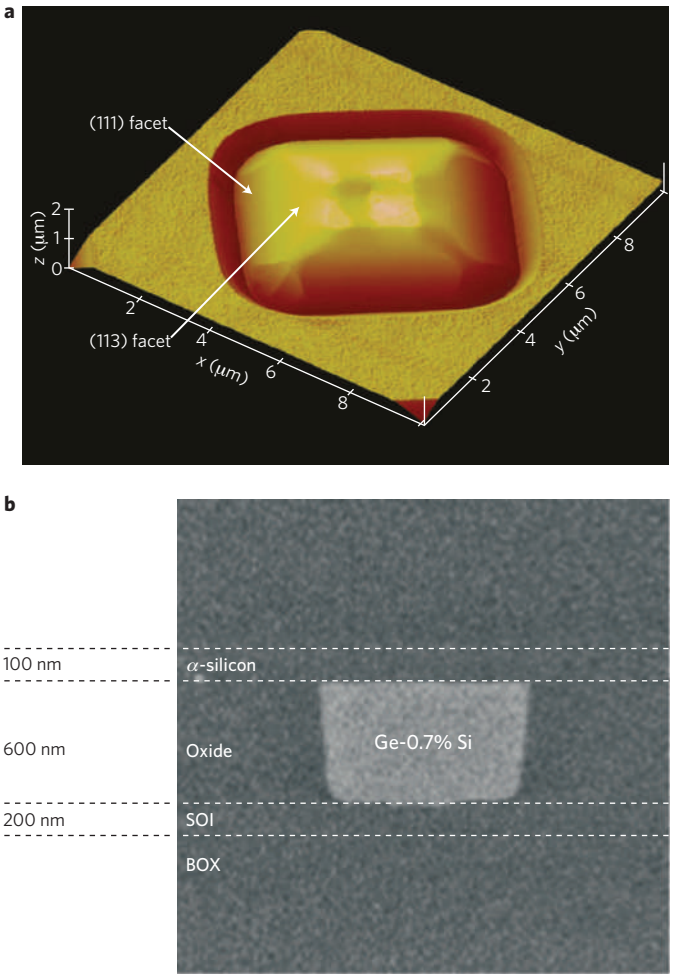

Figure 3 | Selective growth of germanium. a, Atomic force microscope image of a selectively grown Ge mesa in a SiO_2 window. Faceting can be clearly seen at the mesa sidewalls. **b**, Selective, trench-filled Ge. Process-integrated structure of a p-i-n diode using Ge-0.7% Si on a silicon-on-insulator (SOI) substrate. α-silicon, amorphous silicon; BOX, buried oxide. Figure **b** reproduced with permission from ref. 46, © 2008 SPIE.

efficiency of 95% at 1,300 nm for a bias of −1 V. To mask the highly dislocated buffer layer, the detectors were designed as vertical junction devices, with one terminal being the p^+ Si substrate. During the post-growth thermal treatment, boron from the Si substrate diffuses into the highly dislocated Ge buffer layer, making it form part of the bottom terminal. Using an improved device design with vertical n^+-Si/i-Ge/p^+-Si heterojunctions to further enhance the built-in field, an internal quantum efficiency of above 90% in the wavelength range of 650–1,340 nm was achieved at zero bias voltage[33]. At longer wavelengths of 1,500 nm and above, the internal quantum efficiency decreases significantly owing to the smaller absorption coefficient and the limited absorption length defined by the film thickness in the normal-incidence configuration. The internal quantum efficiency can, however, be enhanced by using a resonant cavity. For example, a resonant cavity Ge detector designed for response at 1,538 nm has been used to improve the internal quantum efficiency to 59%[32].

The dark current density of Ge-on-Si photodiodes with thin Ge or SiGe buffer layers is typically of the order of 10 mA cm^{-2}. A notable feature of these photodiodes is that the dark current keeps increasing with applied electric field under reverse bias, and it does not saturate. Temperature-dependent current–voltage data shows that the activation energy for the dark current decreases with

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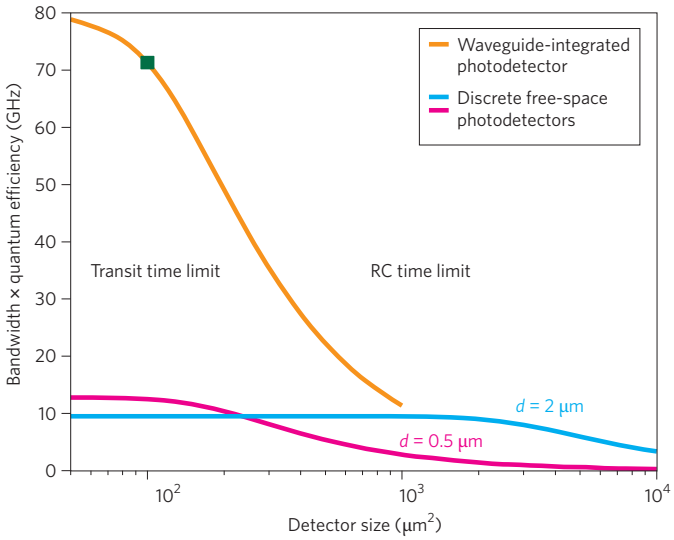

Figure 4 | Product of bandwidth and quantum efficiency as a function of detector area for different Ge detector designs at an operating wavelength of 1,550 nm. Curves for two different Ge thicknesses are shown, highlighting the trade-off between higher quantum efficiency (blue, d = 2 μm) and high speed (pink, d = 0.5 μm), respectively. The green square shows the performance of a 5 μm × 20 μm waveguide-integrated detector with an internal quantum efficiency of 90%.

applied electric field[42], whereas it increases with temperature[43,44]. The authors of these studies conclude that generation and tunnelling processes through defect states in intrinsic Ge under an electric field are the major sources of dark current. Minimizing the operating voltage is therefore desirable for achieving both low dark currents and integration with CMOS circuits.

Several approaches are currently being developed to reduce the dark current density further. Low-temperature Ge buffer layers have been heavily doped with boron to prevent the depletion region from extending into the defective layer, and have also been annealed at high temperature to improve the material quality before intrinsic Ge growth[45]. This approach has been shown to decrease the dark current density to 1 mA cm^{-2}. Ge photodetectors selectively grown to fill submicrometre narrow trenches have demonstrated a dark current density of the order of 0.1 mA cm^{-2} (ref. 46). This technique is highly relevant for waveguide-integrated photodetectors, as will be discussed in the next section. It was recently demonstrated that the dark current density of Ge/Si photodiodes grown by low-energy plasma-enhanced CVD is more than two orders of magnitude lower than devices grown by ultrahigh vacuum or low-pressure CVD with the same threading dislocation density[15]. A dark current density of 4×10^{-5} A cm^{-2} at a bias voltage of −1 V has been achieved in this case, which is approaching that of bulk single-crystal Ge detectors. This result may indicate an effective defect passivation by plasma-introduced atomic hydrogen.

One important performance parameter for photodetectors is their 3 dB bandwidth. Owing to their relatively high carrier drift velocity, Ge photodetectors exhibit fast response times while also showing high responsivity. Table 1 shows the development of detector performance over time for both normal-incidence and waveguide-coupled Ge detectors. The bandwidth of Ge-on-Si photodetectors has been improved from several gigahertz[31,33] to greater than 30 GHz (refs 34,35,37,40,41).

An ideal normal-incidence photodetector would have a high responsivity, low dark current density and high bandwidth. Unfortunately, there are several trade-offs that make such devices difficult to achieve. For example, normal-incidence detectors must be of a reasonable size for fibre coupling; a larger size increases the capacitance and dark current, and therefore also limits the bandwidth and sensitivity. In addition, a large spacing between the anode and cathode reduces the drift velocity of the carriers at a given reverse bias, and therefore limits the bandwidth. Table 1 shows that because of these trade-offs it has so far not been possible to fabricate a normal-incidence Ge detector that simultaneously exhibits high bandwidth, high responsivity and low dark current. Most notably, Ge detectors with metal–semiconductor–metal designs have very high dark currents, most likely due to the poor Schottky contact with Ge.

Ge detectors fabricated on ultrathin silicon-on-insulator substrates have reached bandwidths of up to 29 GHz for operation at 850 nm (refs 9,10). The thin silicon bottom layer made a bottom contact impractical; these detectors therefore featured interdigitated top contacts. For high-speed performance the spacing of the top contacts was optimized for efficient carrier collection, and because of this constraint the Ge thickness was limited by the ability to extend the electric field through the Ge layer and reach saturation velocity for the carriers. This limited Ge thickness and increase in bandgap induced by interdiffusion between the Si and Ge layers resulted in low internal quantum efficiencies at longer wavelengths. These restrictions highlight the limitations common to all free-space detectors in terms of the bandwidth–efficiency product. To increase the speed of these detectors, the Ge layer must be thin to decrease the carrier transit time. On the other hand, a thinner Ge layer absorbs less and so results in a lower photocurrent, particularly in the telecommunications wavelength range of 1,300–1,550 nm.

Waveguide integration

The trade-off between quantum efficiency, bandwidth and a relatively high dark current for free-space detectors can be overcome by using the Ge detector as part of a waveguide. Figure 4 illustrates how the efficiency–bandwidth product depends on the detector size, thus providing a figure-of-merit for detector design. The blue and pink curves show the performance of normal-incidence Ge detectors at 1,550 nm. Two different Ge thicknesses are depicted to show the trade-off between higher quantum efficiency (d = 2 μm) and high speed (d = 0.5 μm). The orange curve shows the theoretical performance of a waveguide-integrated Ge detector at 1,550 nm. Due to the waveguiding nature of the Ge detector, the absorption length is increased and therefore decoupled from the carrier collection path. This configuration allows waveguide-integrated detectors to exhibit high speed while reaching almost 100% quantum efficiency. Furthermore, the device area of a waveguide-integrated photodetector can be almost ten times smaller than that of a free-space detector, so the absolute dark current is significantly lower for the same dark current density. Because noise is determined by the absolute dark current (not the dark current density), waveguide integration also enhances the sensitivity of Ge photodetectors. Dark current density therefore stops being a limiting factor for device performance in such small devices. Table 1 shows that the dark current for waveguide-integrated detectors is generally below 1 μA, with a responsivity of the order of 1 A W^{-1} at 1,550 nm.

The concept of waveguide integration was first successfully demonstrated by Ahn *et al.*[47] using a top-coupled Si_3N_4 channel waveguide. The reported bandwidth–efficiency product of 6.5 GHz at a bias of 0.1 V was already significantly higher than what could be achieved by free-space detection. These results were confirmed by Vivien *et al.*[48], who used a Ge detector coupled to a silicon ridge waveguide.

Three waveguide–detector configurations are possible. The first is to have a waveguide on the top of the Ge detector, with the light coupling evanescently to the Ge detector[47]. The second is to have a waveguide underneath the detector, again with the light evanescently coupling to the detector. However, in this bottom coupled design, the waveguide is made from silicon because the Ge requires a crystalline

Table 1 | Performance comparison for different Ge photodetector designs.

Responsivity (A W^{-1}) @1,550 nm	3 dB bandwidth (GHz)	Dark current density (mA cm^{-2})	Dark current (μA)	Diode design	Year	Reference
Normal incidence design						
0.13 @ 1.3μm, 0V	2.3 @ 3V	0.2	0.2*	p-i-n	1998	4
0.75	2.5	15	0.14*	p-i-n	2002	31
0.035*	38.9 @ 2V	100	0.31*	p-i-n	2005	34
0.56	8.5	10	0.79*	p-i-n	2005	33
—	36.5 @ 2V	1×10^{6}	4×10^{3}*	MSM	2005	37
—	39 @ 2V	375*	0.075	p-i-n	2006	35
0.28	17 @ 10V	180*	0.57	p-i-n	2006	40
0.037	15	27	0.035*	p-i-n	2007	41
Waveguide-coupled design						
1	4.5 @ 3V	0.7*	0.0002	Butt, p-i-n	2006	46,49
1.08	7.2	1.3×10^{3}*	1*	Top, p-i-n	2007	47
1	25 @ 6V	6.5×10^{5}*	130	Butt, MSM	2007	48
0.89	31.3 @ 2V	51 @ 2V	0.17 @ 2V	Bottom, p-i-n	2007	50
0.85	26		3	Bottom, p-i-n	2008	51
1.1	32	1.6×10^{4}*	1.3	Butt, p-i-n	2009	53

The table is divided into normal-incidence devices and waveguide-coupled devices. The references have been listed in chronological order. All performance data are for 1 V reverse bias, unless otherwise stated. The data have been extracted from the references as indicated. MSM, metal–semiconductor–metal. *Data calculated using the referenced material.

template for epitaxial growth[49–51]. The third configuration is to butt-couple the waveguide to the detector, making the detector an extended part of the waveguide[48,49,52]. Both the top- and bottom-coupled detectors exploit the fact that light can be easily coupled evanescently from a lower-index material to a higher-index material as long as the index difference is small. In evanescent coupling, the electromagnetic mode, and hence the optical power, is slowly transferred to the high-index material. Efficient butt-coupling requires mode-matching conditions for waveguide and detector modes. If these are met, the optical power in the waveguide is directly transferred to the detector.

Although butt-coupling is the most efficient coupling mechanism that allows for a very short Ge detector, bottom-coupling is most often used because of the ease of integration into a CMOS process. For applications such as transceivers, limitations on detector size are not severe, which allows for larger devices. Eventually, as more photonic devices are integrated into a single CMOS-based chip, smaller detectors will be needed to increase the density of the photonic devices.

The highest reported efficiency–bandwidth product for a waveguide-coupled Ge detector is 30 GHz at a bias of 1 V (ref. 53). Several Ge detectors with efficiency–bandwidth products of around 20 GHz have been reported, and although these detectors all vary in design, their performances are similar and are generally much higher than normal-incidence devices. There is still a performance gap between the most efficient fabricated diodes and the theoretical limit (Fig. 4). Capacitance and series resistance associated with the metal contacts could be an extrinsic factor that explains the discrepancy in bandwidth between theoretical limit and experimental data.

As mentioned earlier, minimizing the operation voltage of Ge photodetectors is desirable for both dark current reduction and CMOS integration. Optimizing the built-in electric field in the intrinsic Ge layer by adequately controlling the doping profile in a p-i-n diode structure enables full responsivity for photovoltaic operation at zero bias[33,47,51]. In recent years, bandwidths at zero bias have also been improved significantly, particularly for waveguide-integrated devices, because the thickness or width of the intrinsic Ge region can be reduced to obtain a stronger built-in electric field at zero bias for vertical or lateral p-i-n structures, respectively, without affecting the optical absorption path length in the longitudinal direction. For example, Ahn *et al.*[47] reported a bandwidth of 6.6 GHz at zero bias, which is nearly 90% of the full bandwidth at a reverse bias of −3 V. Yin *et al.*[50] and Feng *et al.*[53] reported bandwidths of 16 and 17.5 GHz at zero bias, respectively. Photovoltaic operation at zero bias is especially beneficial for achieving high energy efficiency in large-scale electronic–photonic integration because the photodetectors consume almost no power at all.

CMOS integration

There are several approaches to integrating Ge detectors into a CMOS process. Because Ge is already in use at the 'front end of the line' (the first stage of integrated circuit fabrication), a straightforward approach is to insert the Ge epitaxy step in an established CMOS process flow after poly-gate formation and before contact module or metallization. This approach was successfully demonstrated by Luxtera in a 130 nm CMOS technology node[39] and by the Massachusetts Institute of Technology in collaboration with BAE Systems in a 180 nm node[46]. Although the performance of these detectors was sufficient for the applications for which they were developed, optimization of the device for more advanced CMOS technology nodes is limited by the fixed layer thicknesses and process flow. It would be desirable to have access to a CMOS process that could be adapted to optimize electronic as well as photonics devices. Unfortunately, such a process is not currently available, and the main limitation lies in the access to pure Ge growth. Foundries usually have access to SiGe growth with up to 50% Ge. In many cases, wafers are shuttled from a foundry, where the transistor level is fabricated, to a fabrication plant with Ge growth capability, where the metallization is performed. There are several ongoing projects to achieve the integration of Ge detectors in a single fabrication laboratory.

It would be ideal to integrate Ge photodetectors with 'back end of the line' processes (in which active components are interconnected with wiring on the wafer) in the upper interconnect levels, such that these photonic devices do not compete with CMOS transistors at the single-crystalline-Si level. However, growing high-quality Ge on amorphous layers poses a significant challenge in such cases, and research in this area is still at an early stage. Development of Ge

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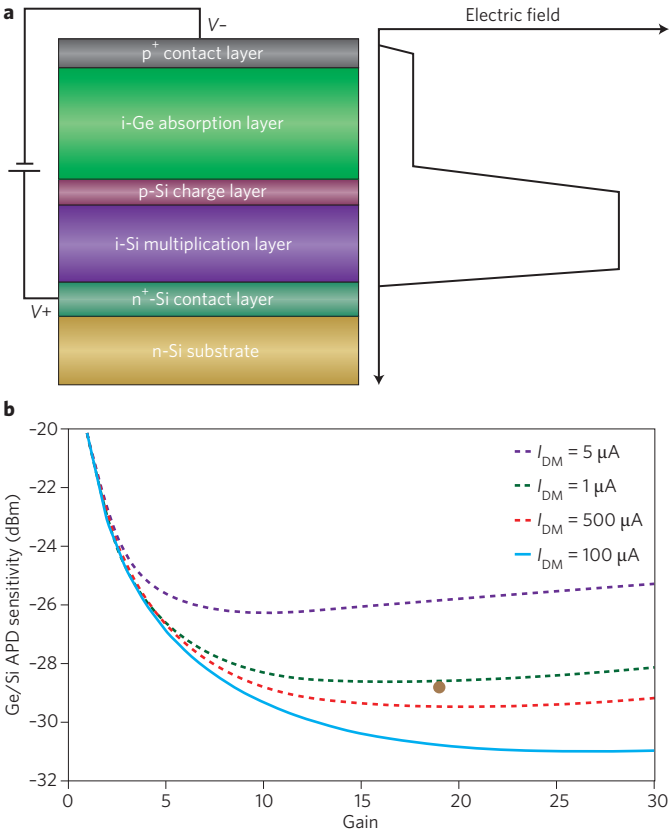

Figure 5 | Ge/Si APD design and performance. a, Schematic cross-section of a Ge/Si APD with a SACM structure and its internal electric field distribution. **b**, Theoretical 10 Gb s^{-1} Ge/Si APD receiver sensitivity at a bit-error-rate of 10^{-10}, wavelength of 1.31 μm and an ionization ratio of k = 0.1, as a function of gain for different primary dark currents, I_{DM}. A responsivity of 0.5 A W^{-1} and typical transimpedance amplifier input-referred root-mean-square noise of 1 μA is assumed. The brown dot in **b** shows the Ge/Si APD receiver measurement from ref. 56, which is in good agreement with the theoretical model.

photodetectors on dielectric or amorphous-Si layers for low fabrication temperatures has been reported[54–57]. There are also efforts to develop submicrometre Ge photodetectors through integration with near-infrared dipole antennas, potentially achieving bandwidths of >100 GHz at very low power consumption[58]. Incorporating Ge epitaxy after poly-gate formation and before metallization will remain a dominant solution for CMOS integration in the near future.

Avalanche photodetectors

Avalanche photodetectors (APDs) are widely used in high-bit-rate, long-haul optical communication systems. Compared with their p-i-n counterparts, APDs offer ~5–10 dB better sensitivity due to their internal multiplication gain[59]. Ge/Si APDs combine the excellent optical absorption of Ge at telecommunications wavelengths with the outstanding carrier multiplication properties of Si. In the high-electric-field gain region of Si, photogenerated electrons from the Ge absorption layer undergo a series of impact ionization processes, which consequently amplifies the photocurrent and improves the sensitivity. The key figure of merit of a multiplication material is the ionization ratio k, which is defined as the ratio of the multiplication rate of one carrier type to the other, such that the value is less than 1. This parameter affects the excess noise, the gain–bandwidth product, and thus the sensitivity of an APD[59]. Ideally k should be minimized such that the multiplication process is dominated by either electrons or holes to reduce excess noise and increase the bandwidth. Si has a much smaller k (<0.1) than typical multiplication materials used in group III–V APDs such as InP (k ~ 0.5), making it more advantageous for use as a multiplication layer. By combining the success of epitaxial Ge diodes with a highly desirable Si gain region, Ge/Si APDs promise to be a competitive candidate in high-speed optical communication systems with higher gain–bandwidth products and better sensitivity over traditional group III–V APDs. The high performance and monolithic CMOS integration capability can also expand the application of Ge/Si APDs to other fields, such as 3D imaging and single-photon detection[60].

Ge/Si APDs have a separate absorption-charge-multiplication (SACM) structure, in which light is absorbed in an intrinsic-Ge (i-Ge) film and electrons are multiplied in an intrinsic-Si (i-Si) film. Figure 5a shows a cross-sectional view of a Ge/Si APD with a SACM structure, together with its internal electric field profile. SACM structures allow the i-Ge and i-Si films thicknesses to be chosen separately to optimize both quantum efficiency and multiplication gain. The i-Si film thickness is chosen by considering the gain–bandwidth product and sensitivity; at a lower gain, the bandwidth is mainly limited by the resistance–capacitance delay and transit time, but at higher gain the time required for avalanche build-up associated with the high gain coefficient becomes more significant, which further reduces the bandwidth[61]. Another trade-off is between gain and sensitivity. Higher gain increases responsivity, yet it also increases multiplication noise. Optimal i-Si thickness is determined by the optimal gain at the operating voltage. The key design parameter is the internal electric field distribution in the i-Ge and i-Si films, and this can be controlled by varying the charge density σ_{charge} of the p-Si charge layer in between the i-Ge and i-Si layers. The goal of optimizing σ_{charge} is to ensure that the electric field intensity in the i-Si film is sufficient to achieve effective avalanche multiplication but is still below its tunnelling threshold (which is typically of the order of several hundred kV cm^{-1}), while simultaneously keeping a moderate electric field of several kV cm^{-1} in i-G, such that a high carrier drift velocity is achieved without significantly increasing the tunnelling current. An optimized value of σ_{charge} is typically of the order of 10^{12} cm^2, and it can be varied depending on the intrinsic carrier concentration in the i-Ge and i-Si layers.

Ge/Si APDs were recently successfully fabricated through both blanket epitaxial Ge growth[62] and selective Ge growth on epitaxial Si films[63]. During Ge/Si APD fabrication, a 50–100 nm p-Si charge layer can be formed either by ion-implantation into the epitaxial i-Si layer or by *in situ* doping. Other processing techniques are similar to the Ge p-i-n diodes discussed earlier.

Although the gain–bandwidth product is commonly used in literature to characterize APD performance, sensitivity is a more complete figure of merit that reflects the gain–bandwidth product, responsivity, excess noise and dark current. Figure 5b shows the theoretical sensitivity of 10 Gb s^{-1} Ge/Si APDs at a bit-error-rate of 10^{-10} as a function of gain for different primary dark currents (I_{DM}) using the model given in ref. 66. This figure assumes a primary responsivity of 0.5 A W^{-1}, a typical transimpedance amplifier noise of 1 μA, and that the input optical power at the 'off' state is negligible compared with that at the 'on' state. Clearly at a dark current of <1 μA and a gain of >10, Ge/Si APD receiver sensitivity is theoretically better than commercial group III–V APD receivers (from −28 to −26 dBm). The measurement data of a Ge/Si APD receiver from ref. 62 is also shown in Fig. 5b, in which the primary dark current is ~500 nA. The measured sensitivity of −28.7 dBm agrees well with the theoretical value of −29.5 dBm.

There are at two approaches for improving Ge/Si APD sensitivity: either reduce the primary dark current below 100 nA, or enhance the primary responsivity to the commercial group III–V

APD level (>0.8 A W^{-1}). Similar to waveguide-coupled Ge p-i-n diodes, waveguide-integrated Ge/Si APDs offer advantages in their low absolute dark currents and high bandwidth–efficiency products. Recent waveguide-integrated Ge/Si APDs have successfully demonstrated sensitivities of −31 dBm and bit-error-rates of 10^{-10} at a wavelength of 1.3 μm (ref. 65).

Future outlook

Ge photodetectors have advanced rapidly with the development of direct epitaxial growth of Ge on Si. Today, fully CMOS-integrated Ge photodetectors are commercially available in transceivers for optical communications[51,66] and in CCD arrays for near-infrared imaging[67]. The performance of Ge photodetectors is now comparable to or even exceeds the performance of InGaAs photodetectors, which are commonly used in telecommunications applications.

Ge photodetectors have revolutionized both silicon technology and optical communications by bringing shorter absorption lengths, higher electron mobilities, faster response times and lower power dissipation. Epitaxial integration on submicrometre-scale silicon waveguides allows an input optical coupling efficiency of nearly 100% with a small device size, and a corresponding low capacitance and dark current. The density of states of Ge is slightly higher than in competing group III–V photodetector materials, and the theoretical dark current is slightly higher. Because dark current is a direct determinant of noise, this factor was once considered to be significant. However, waveguide integration affords a dimensional scaling path to disruptive, small-area detectors with ideal responsivity, low dark current and low noise. The net impact of monolithic, CMOS-integrated photodetectors is that they essentially offer higher yields, lower noise and faster response times than any other competing technology, at no incremental cost.

The path for Ge photodetector technology is being driven by rapid architectural changes in applications[68]. On-chip receivers connected to optical fibres by free-space coupling will achieve pervasive market penetration within the next five years. This technology is single-channel, involves multimode transport, and is based on vertical-cavity surface-emitting laser design, which makes detector area an important factor that limits the device speed.

The single-channel multimode optical cable will remain dominant for the next decade, with data rates of 10–25 Mbit s^{-1}. This performance level fits comfortably within the commercially demonstrated capability of discrete Ge photodetectors. When bandwidth density requirements dictate a single-mode wavelength-division multiplexed solution, the benefits of waveguide integration will be used to their full advantage. Parallel system architectures allow performance to be increased at constant clock frequency simply by adding more nodes. Beyond around 16 nodes a parallel system can no longer function efficiently with electrical interconnections. Therefore, scaling to thousands of nodes will require optical interconnects and wavelength-division multiplexing to achieve sufficient bandwidth densities. Because the detector count scales as the square of the node count, waveguide-integrated nanostructured Ge-on-Si detectors with subfemtofarad capacitance will be needed to achieve high performance, high power efficiency and programmability.

Germanium operates in the eye-safe spectral region of around 1,500 nm, allowing these elements to be safely deployed throughout human environments. Potential examples are for motion sensors, fire detectors, and light detection and ranging (LIDAR) control systems for automobiles.

Ge-on-Si photodetectors will be rapidly deployed into dense, on-chip environments when single-mode optical signalling is adopted. Such architectures will probably use an optical power bus with multiple wavelengths and synchronization channels. Filters will load optical channels onto a data bus that will encode using local modulators. The optical power supply can be off-chip, and may ultimately be as simple as a wall plug. Initially, the optical plane will be incorporated by chip stacking or other methods achievable through silicon technology. Ultimately, monolithic integration in the chip interconnect stack will be implemented. The challenge for Ge-on-Si detectors will be to achieve high performance without resorting to the benefits of epitaxy. Ge photodetectors fabricated at low temperatures (<450 °C) will be required for back-end-of-line CMOS applications, and the small size of the detectors at this point will facilitate the device development.

We envision that low cost, integrated Ge-on-Si photodetectors will enable a range of new capabilities from high-end advanced modulation format transmission to coherent and optical heterodyne detection. The performance of these photodetectors continues to make positive progress, and the future is rich with opportunity.

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Additional information

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